

# 3D Simulation of high-speed serial interface design

*by*

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# Objective



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- Package contains a test chip used as physical layer implementation of a high-speed serial link.
- Investigations have to be performed with the help of a 3D electromagnetic solver - CST Microwave Studio 5 -.



# State of the Art



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# State of the Art

Background



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- Increasing demand for high bandwidth data communication leads to



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- Increasing demand for high bandwidth data communication leads to
  - ever increasing interface frequencies.
  - higher number of I/O pads.
- Systems becoming smaller leads to
  - packages with higher complexity.
  - closely spaced interconnects and narrow pitch interval.



# Consequences



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- High speed data rates, I/O density and tight geometries create parasitic effects like crosstalk, attenuation and reflections.



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- Direct measurements with Time - domain Reflectometry (TDR) techniques.



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## Electrical Characterization

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- Direct measurements with Time - domain Reflectometry (TDR) techniques.
- **Computation of electric and magnetic fields using 3D field solver tools.**



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# Modeling and Simulation Procedure



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# Modeling and Simulation Procedure

Chip Package  
Geometrical  
Model

- Obtaining the package layout containing information regarding geometries and material parameters for the compound and first and second level interconnects.



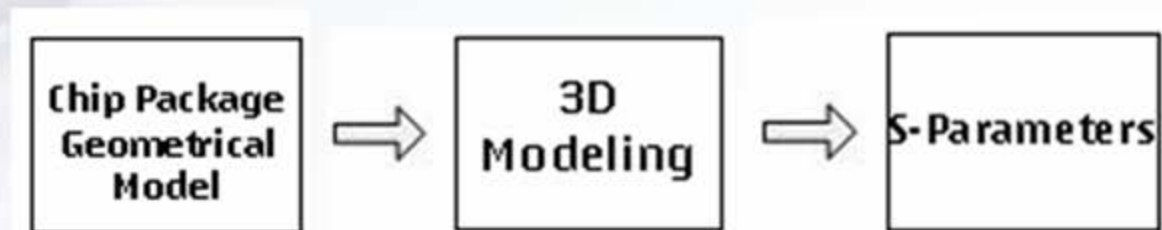


# Modeling and Simulation Procedure



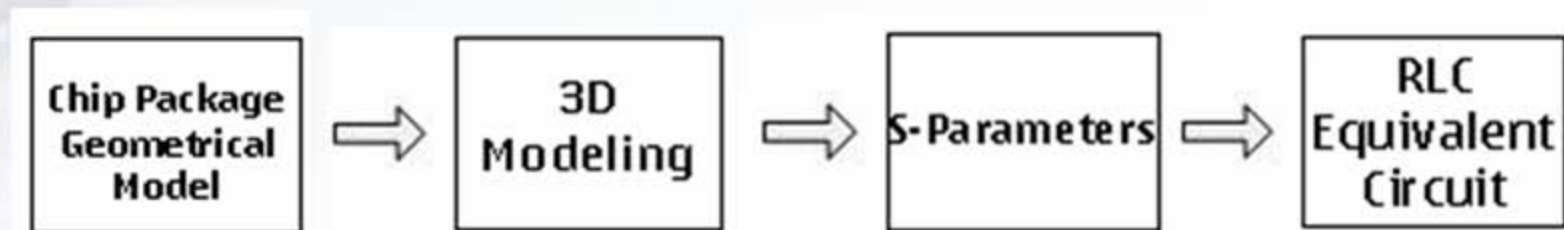
- Building the 3D model in CST MWS.

# Modeling and Simulation Procedure



- Time- and Frequency simulators used to generate s-parameters.

# Modeling and Simulation Procedure



- Deriving SPICE compatible network model consisting of lumped R,L,C,G,K elements.

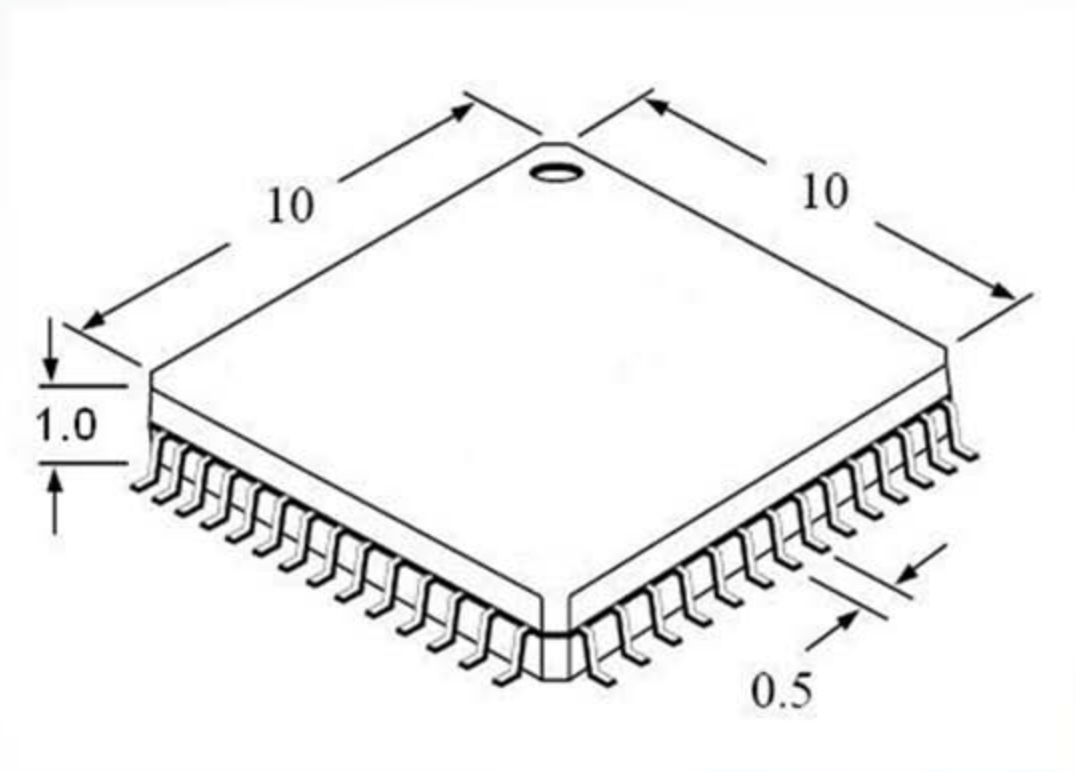
# Modeling and Simulation Procedure



- Including the equivalent circuit into circuit simulator to identify the input of the package parasitics on the signal integrity.

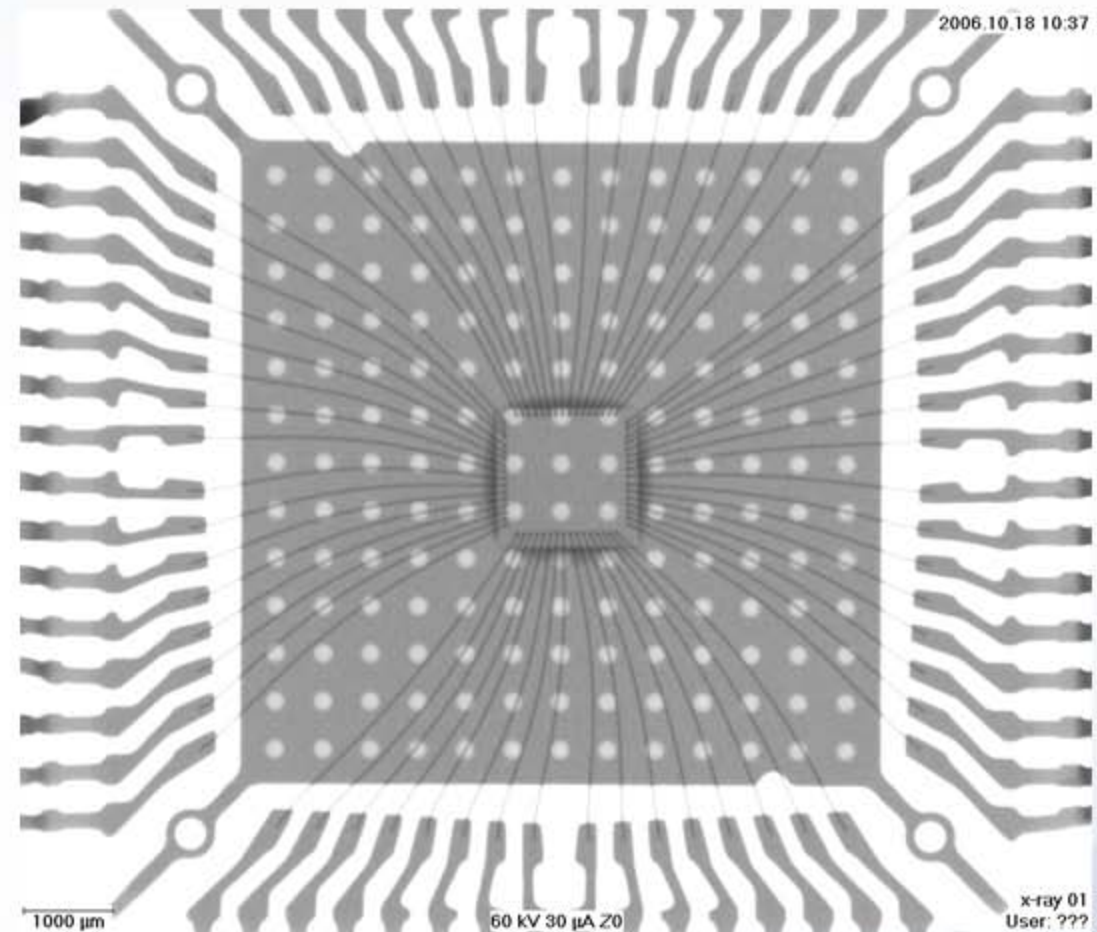
# Test Chip Package

- Package is 10x10 mm<sup>2</sup> small with body thickness 1 mm
- 1.4x1.4 mm<sup>2</sup> small IC with an active area of 0.01 mm<sup>2</sup> is mounted concentrically on silicon substrate
- Gold bond wire diameter is 20 μm with bond pad pitch of 70 μm
- Gull-wing shaped copper leads with lead pitch 0.5 mm



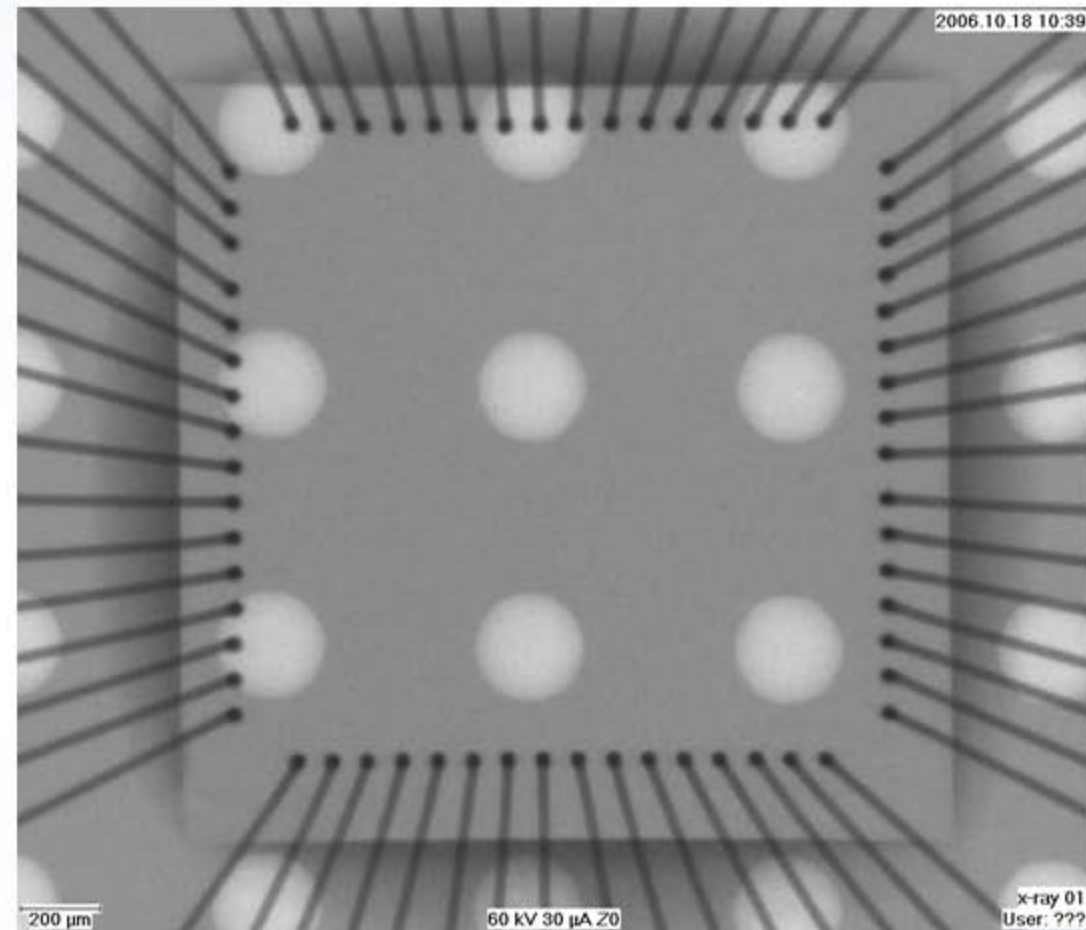
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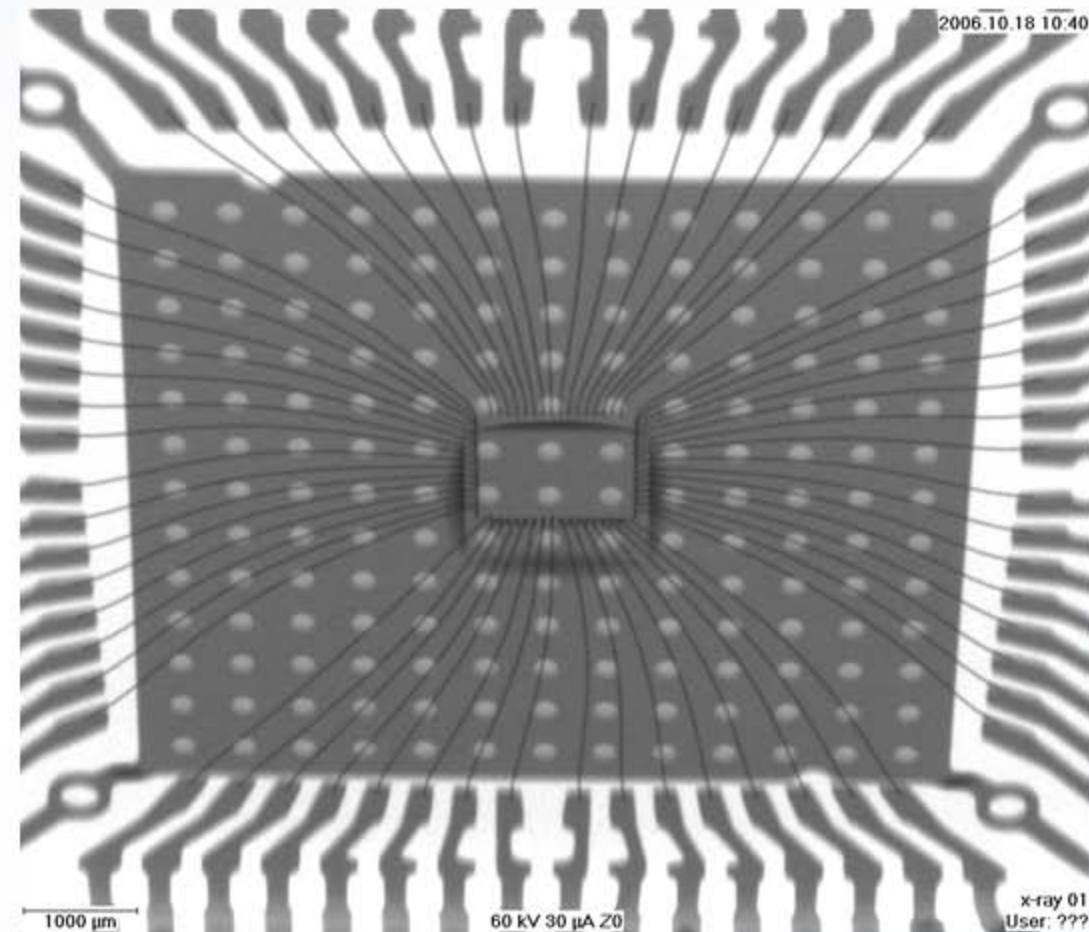
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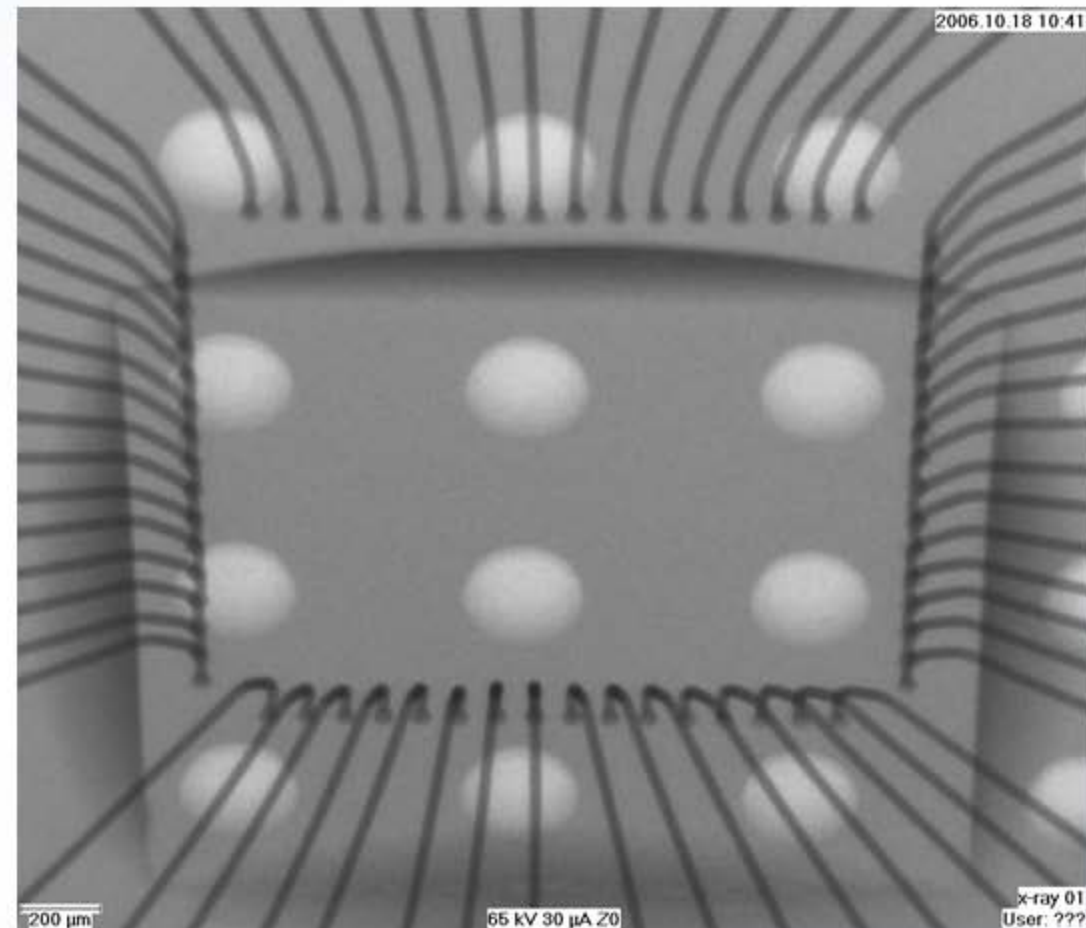
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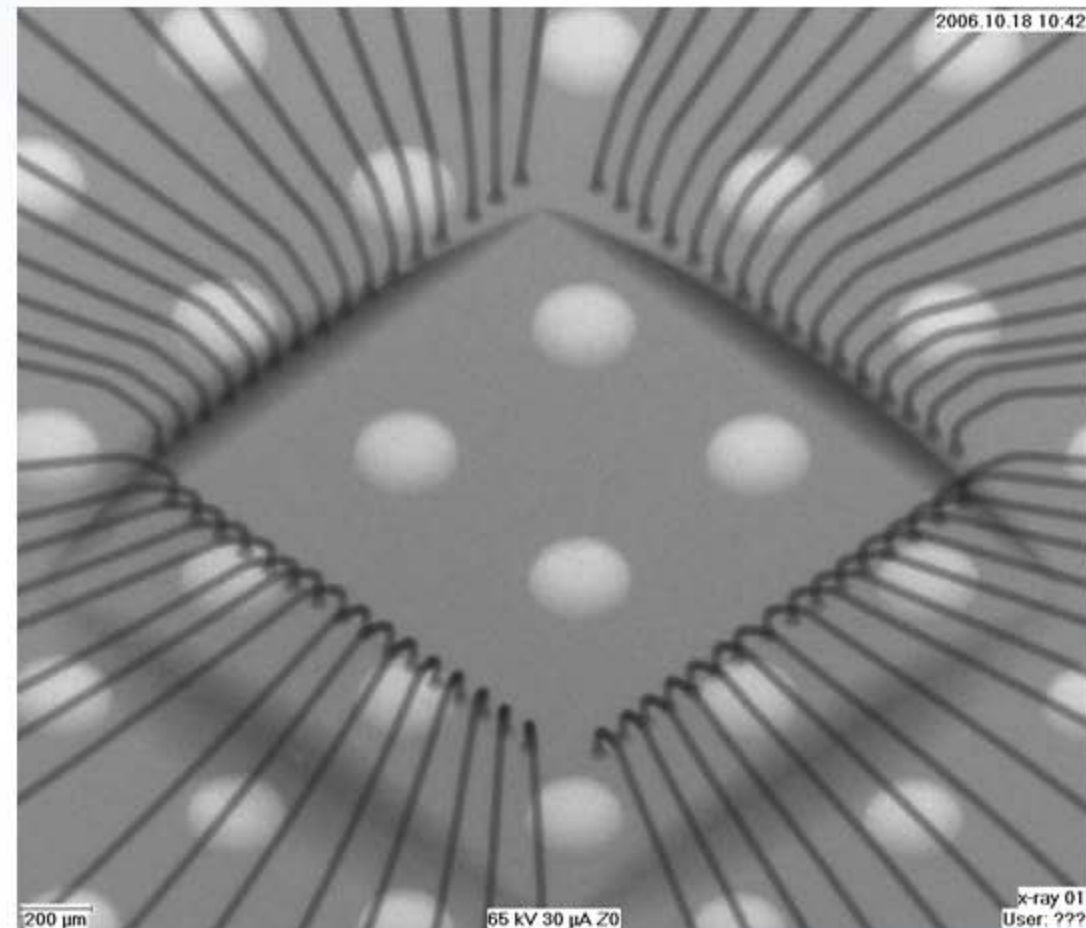
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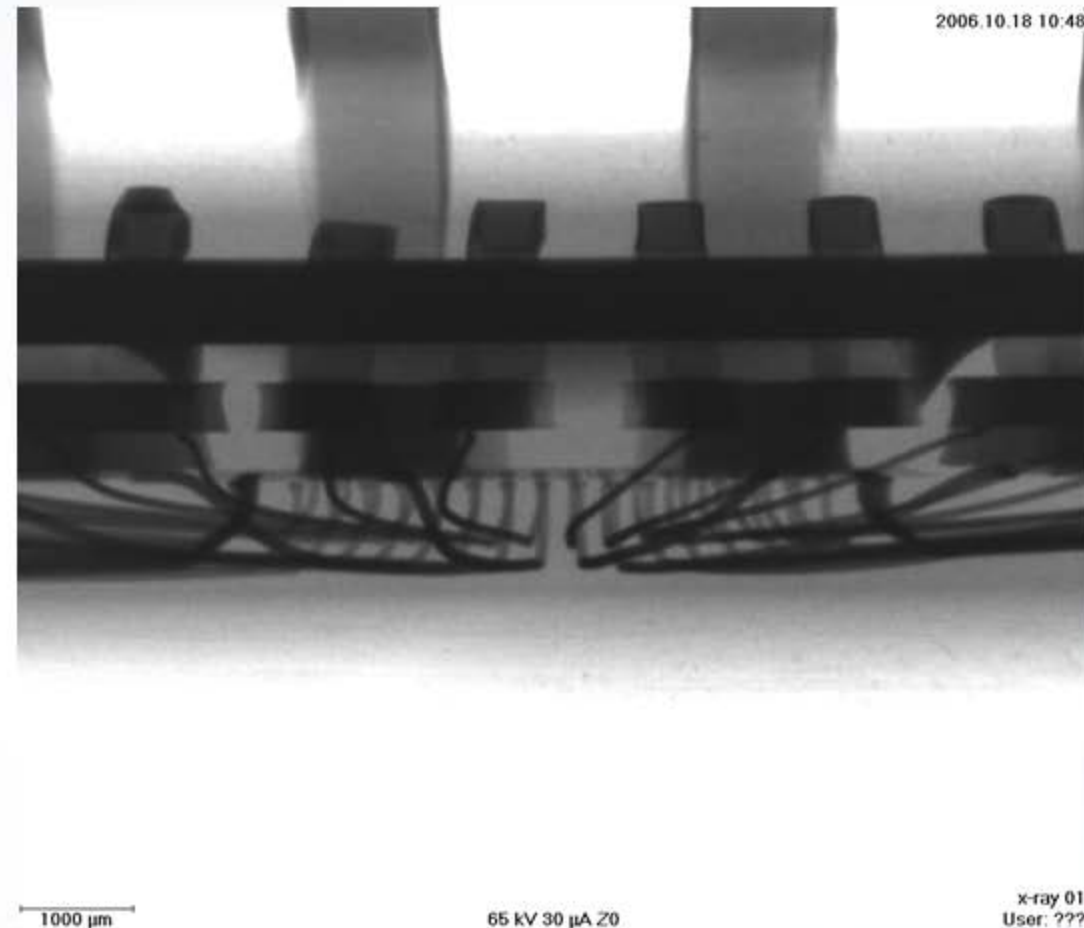
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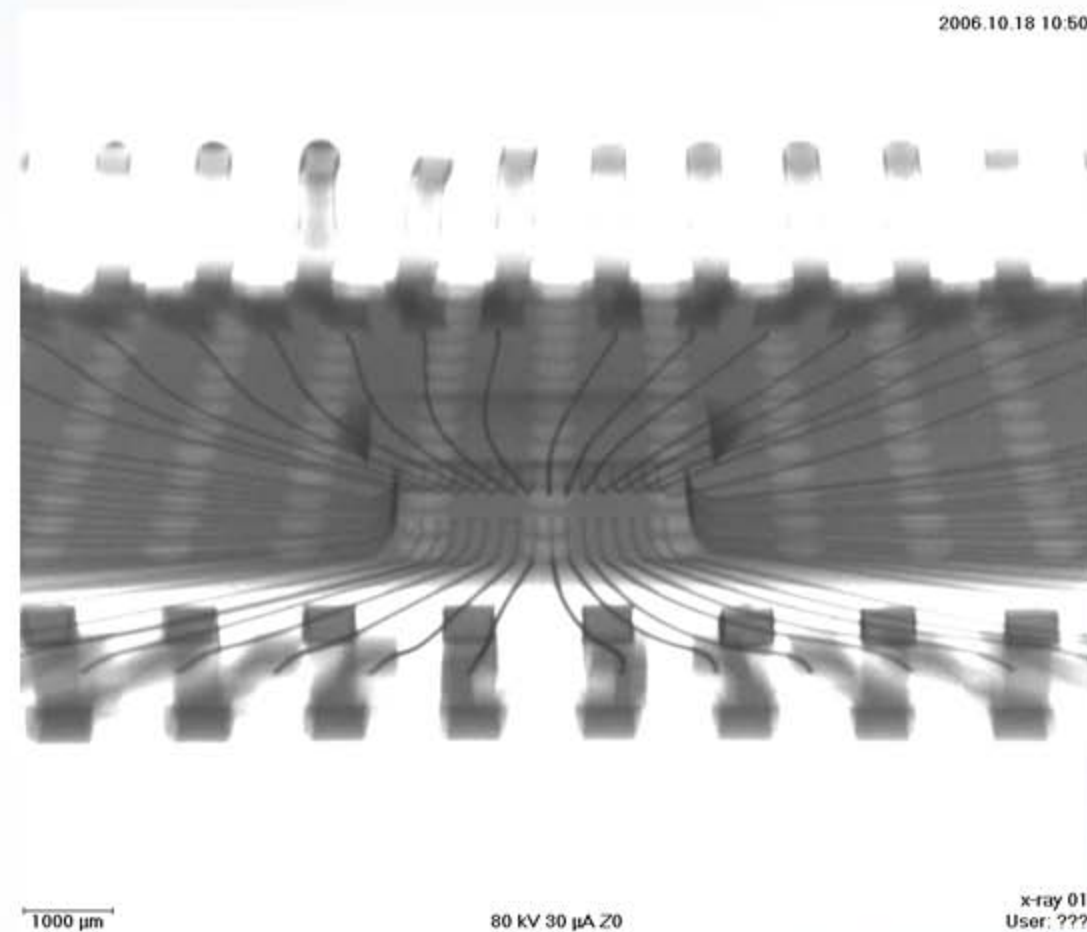
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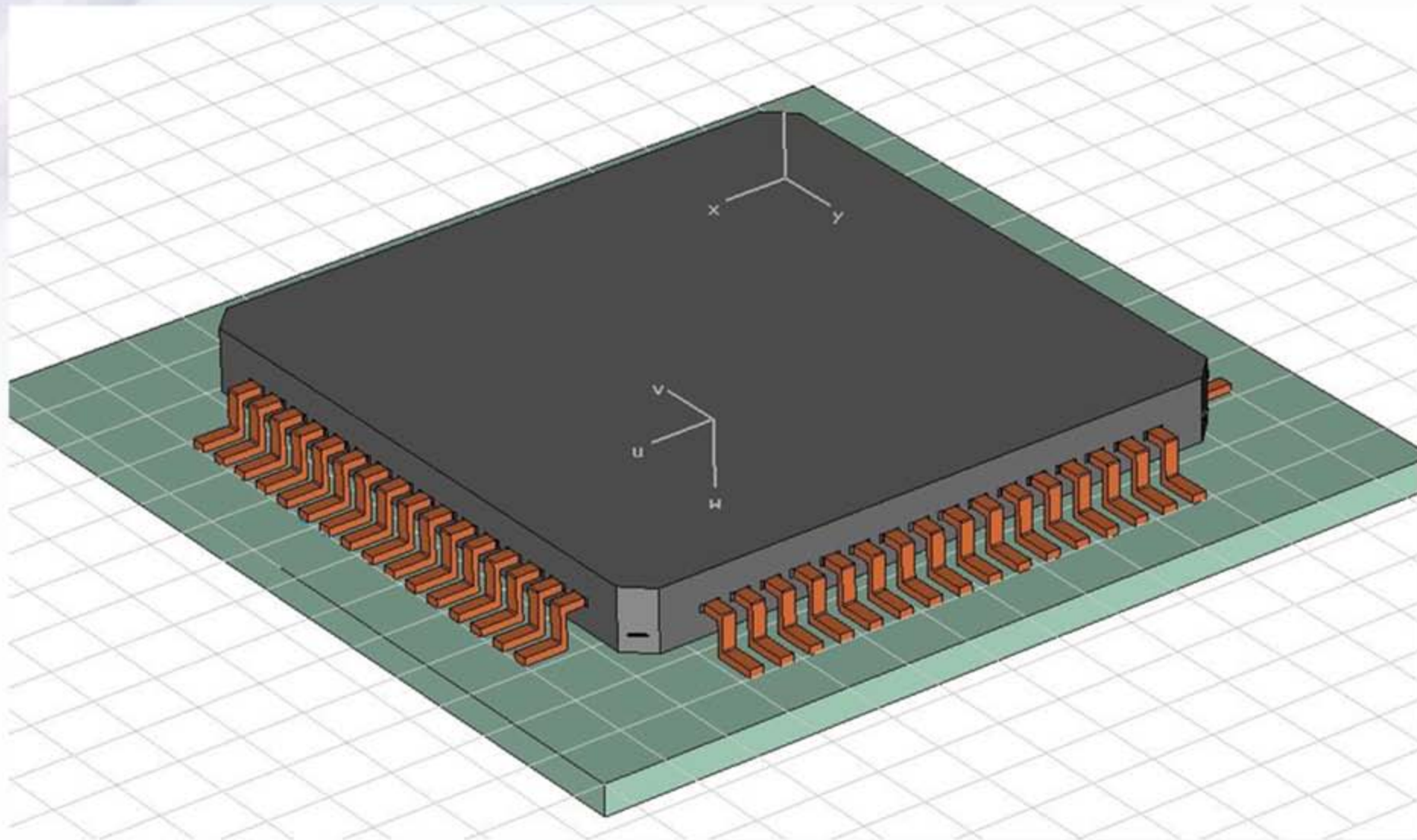


# 3D Model

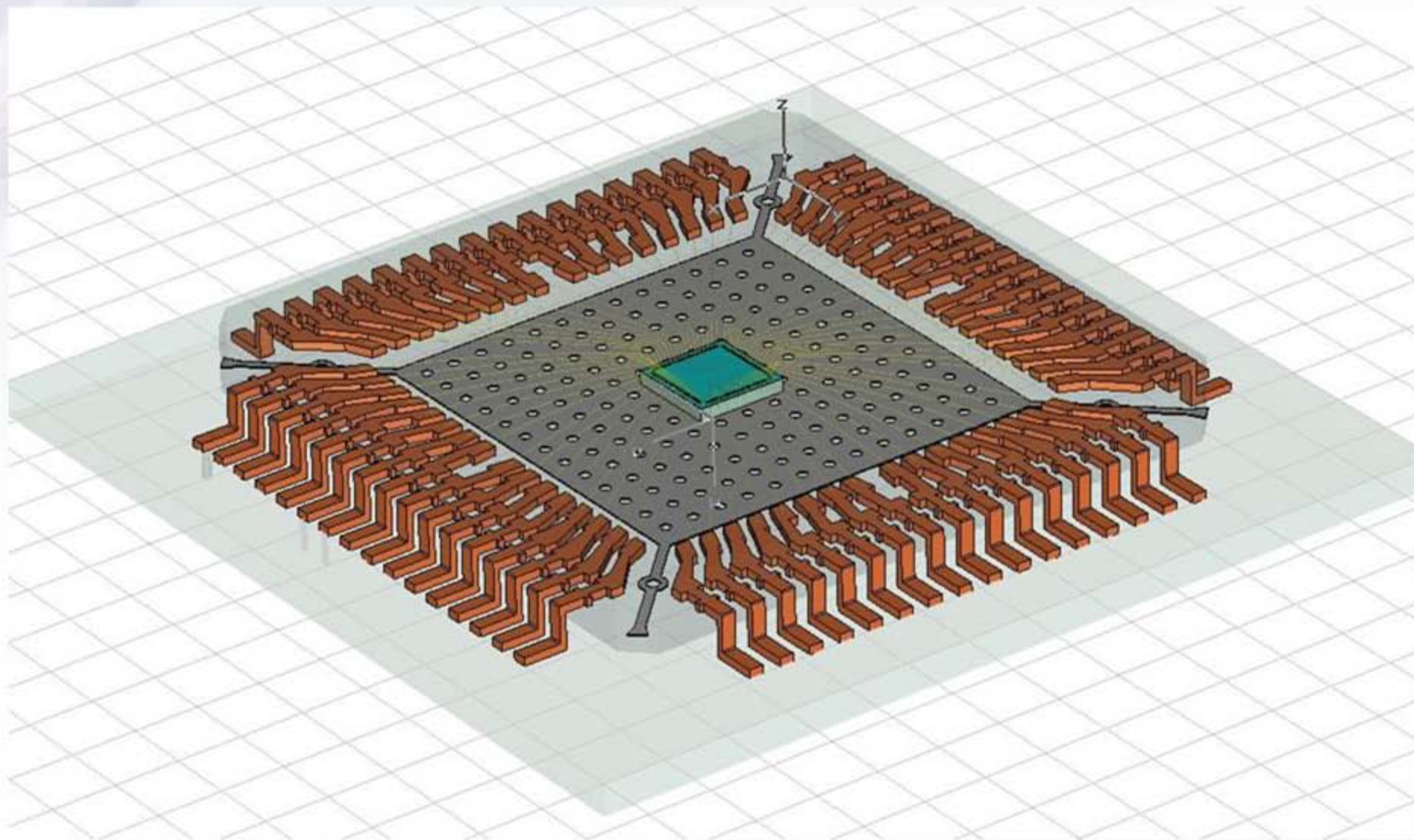


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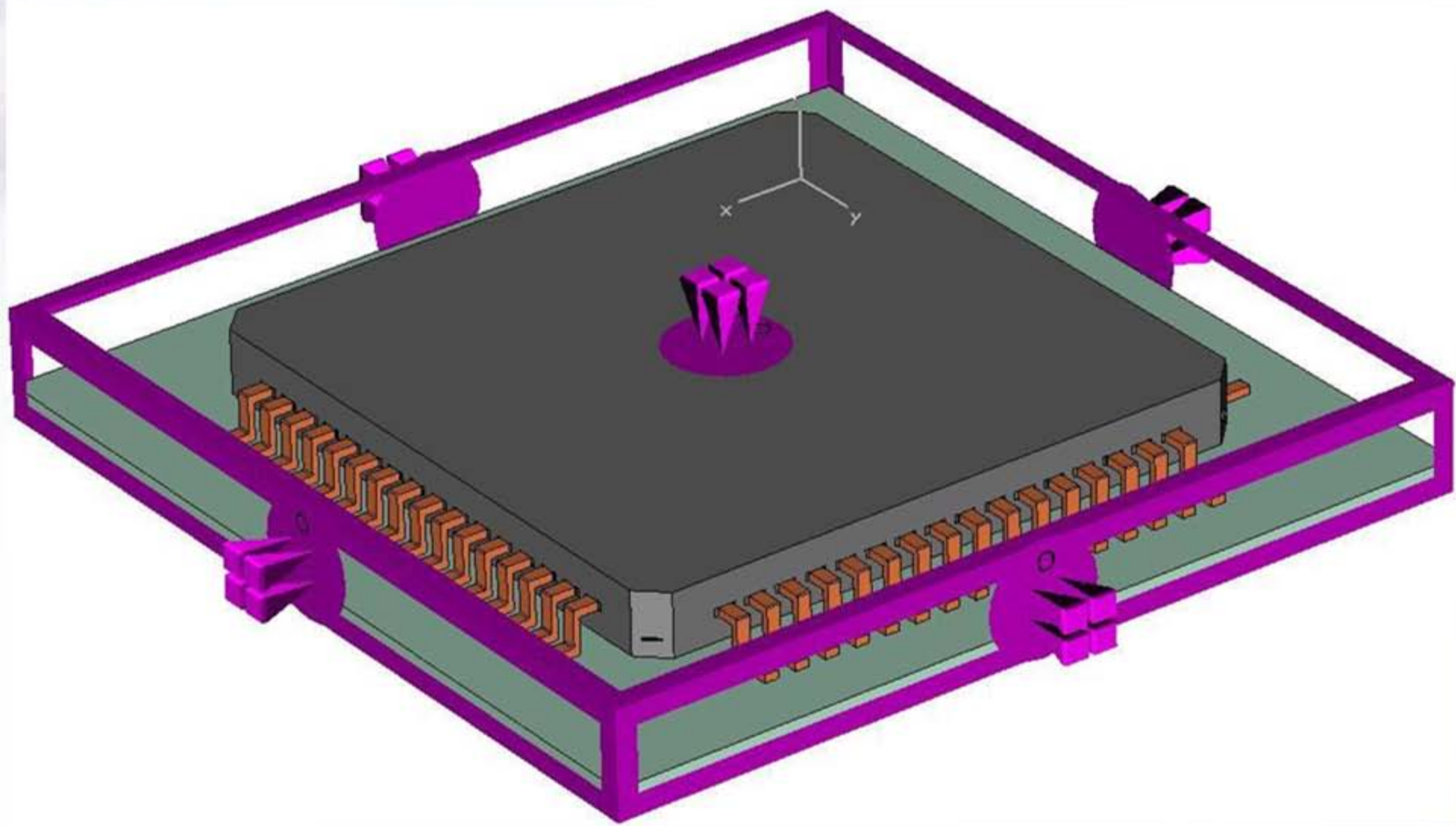


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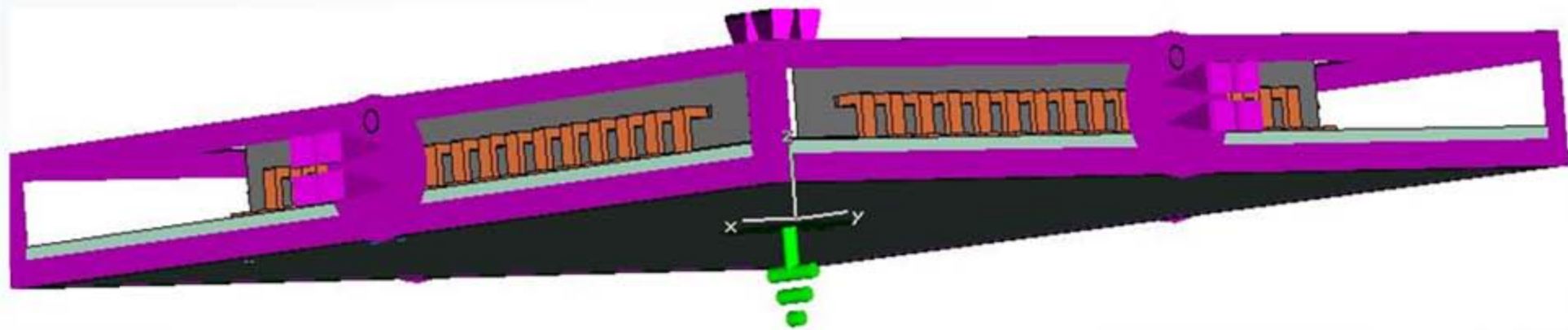




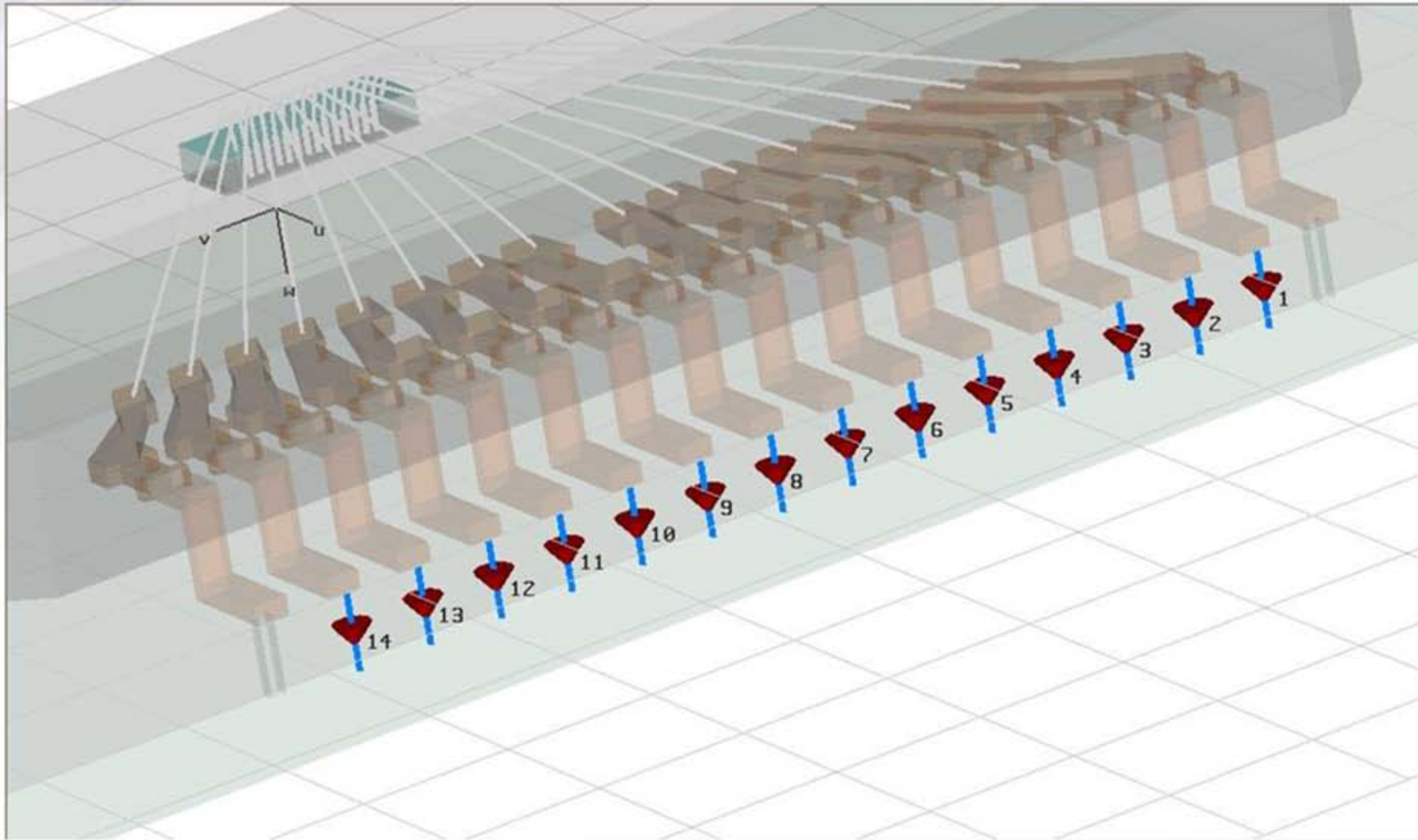
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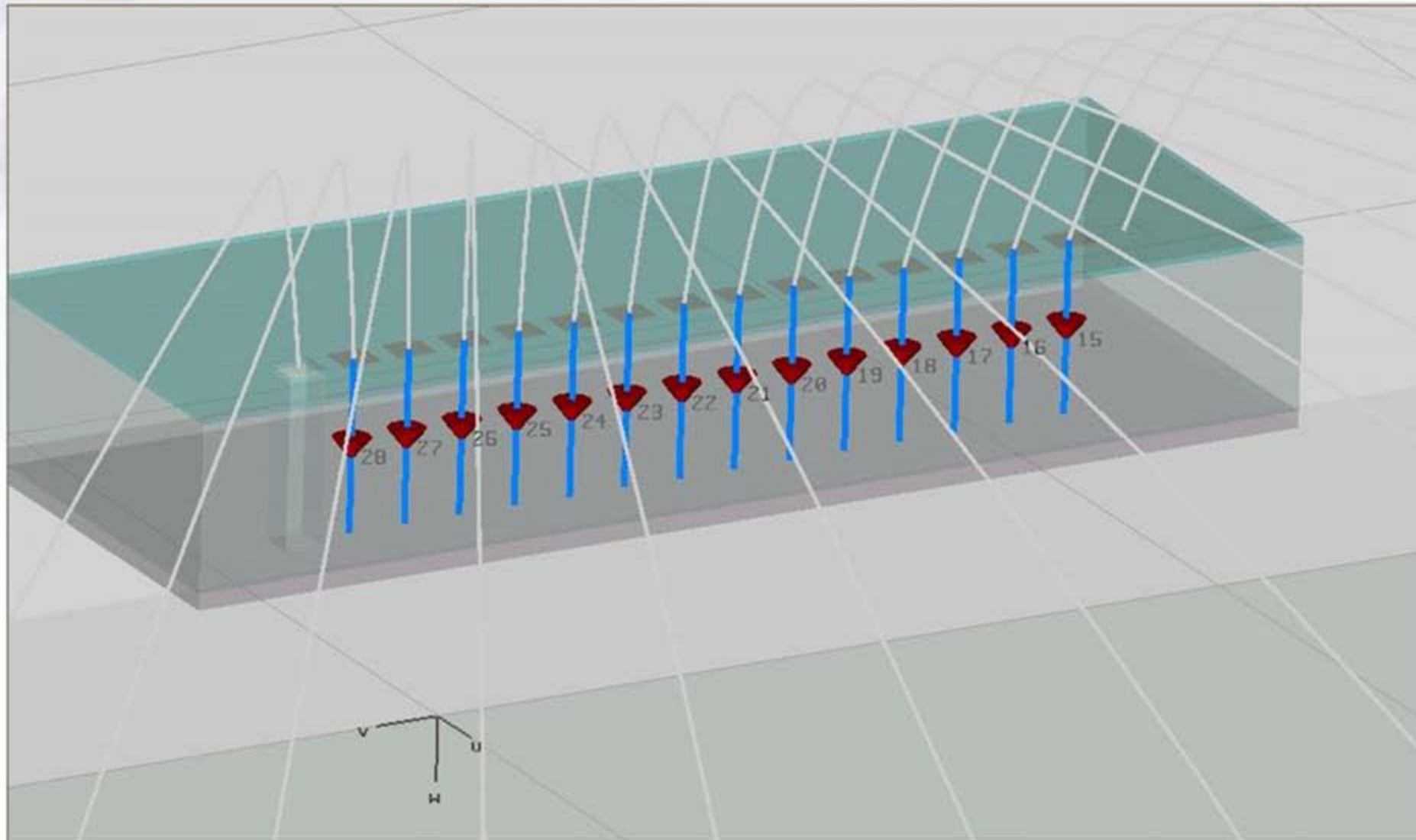
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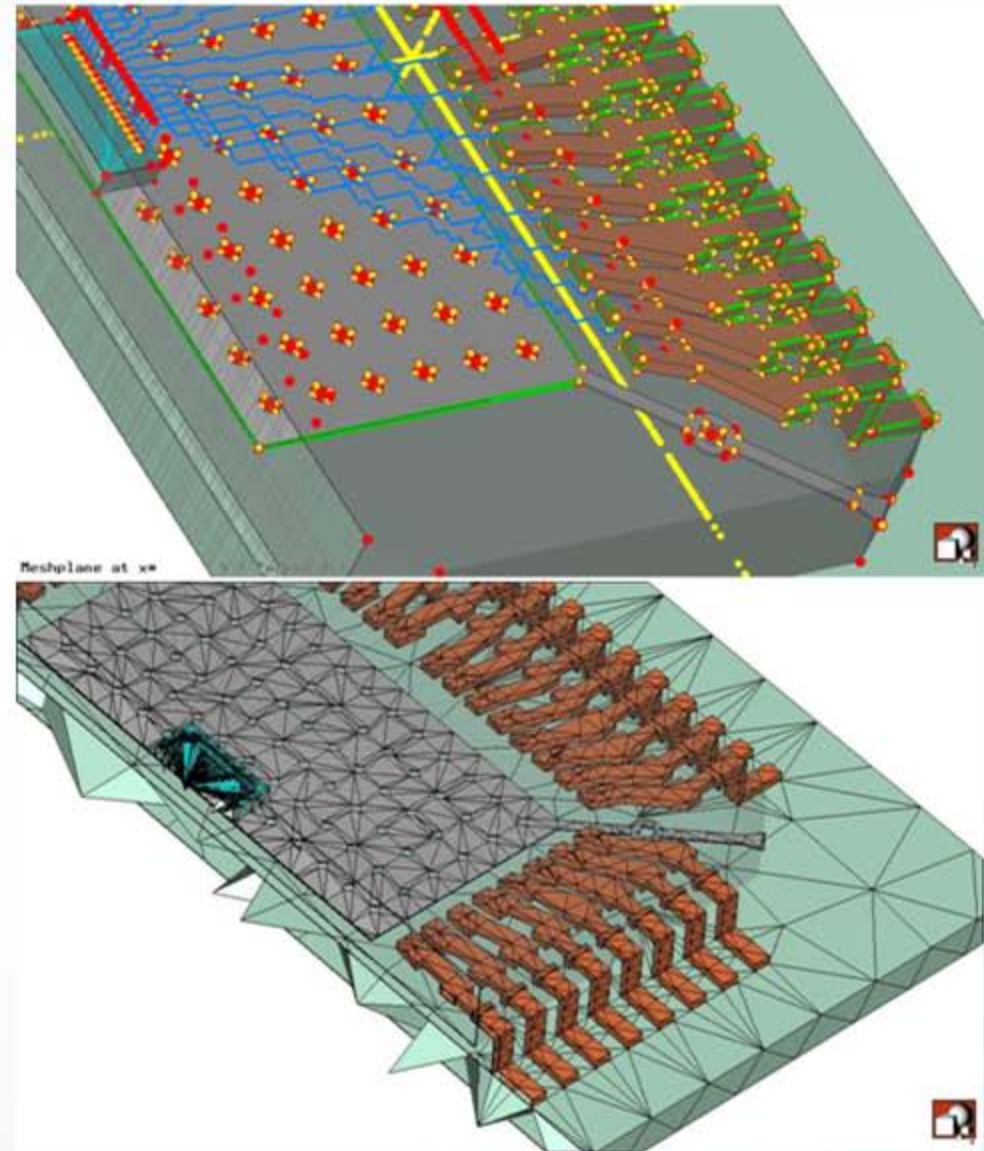


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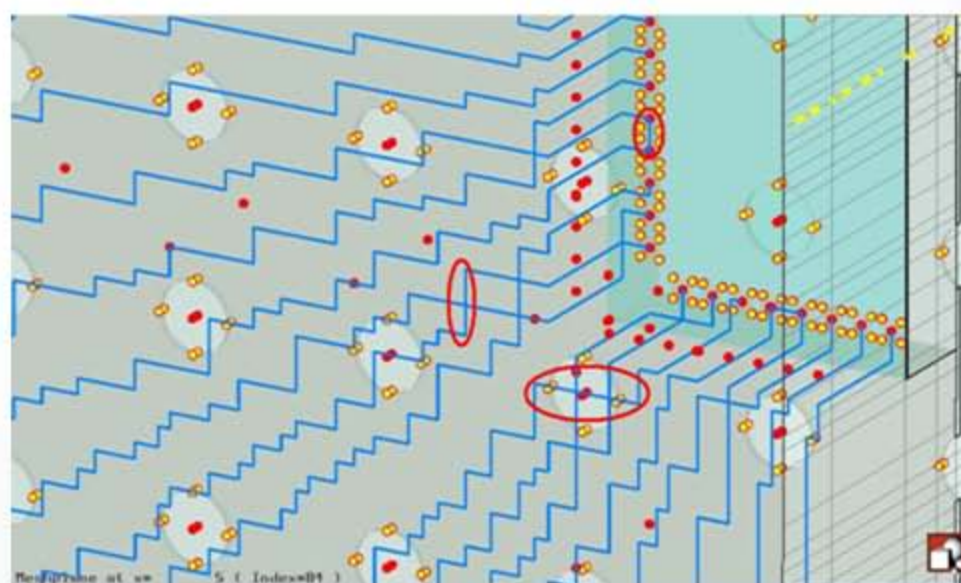
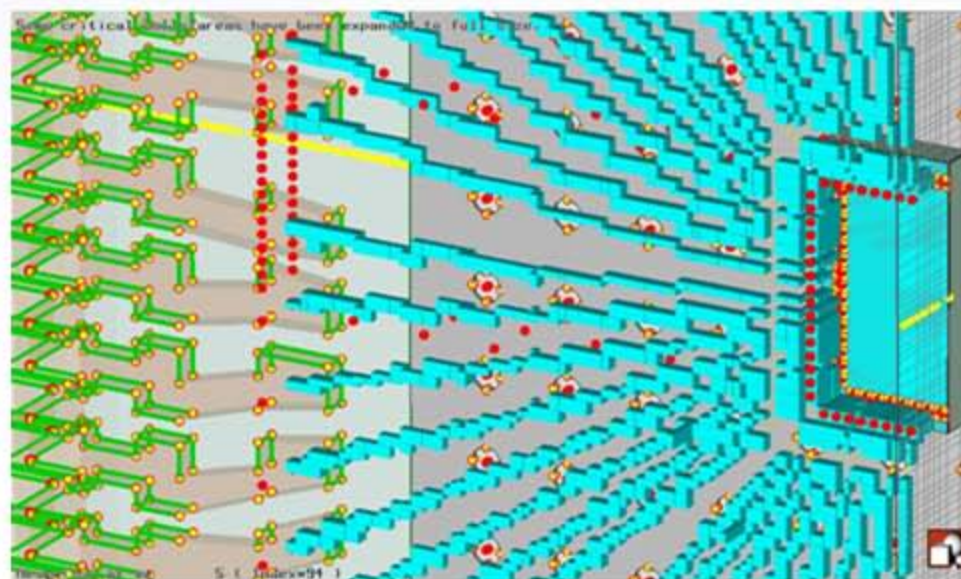
# Meshing

- To calculate electromagnetic properties, the structure has to be discretized
- Two different mesh types were utilised; hexahedral and tetrahedral
- Mesh density for both types can be generated automatically, adaptively or manually
- Finer mesh will lead to more precise values



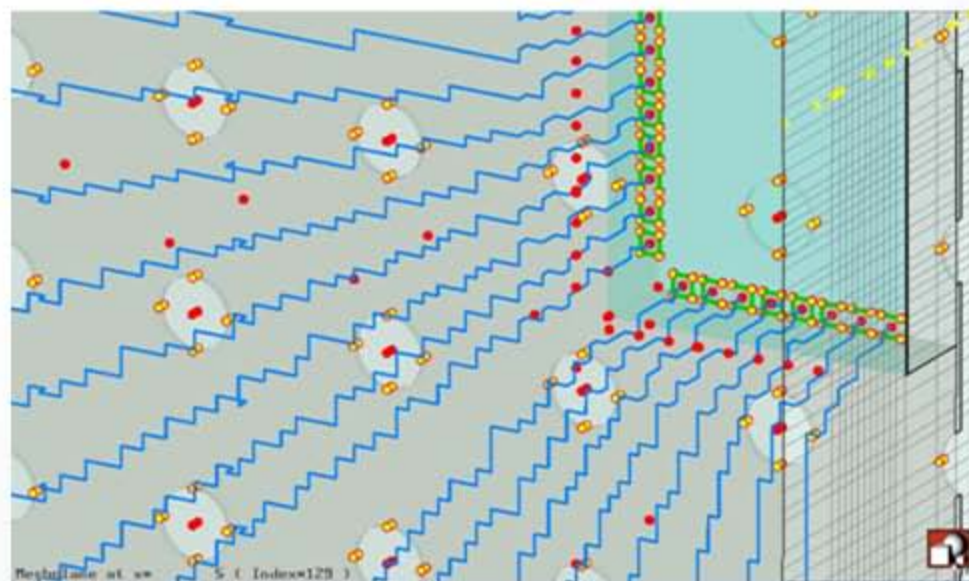
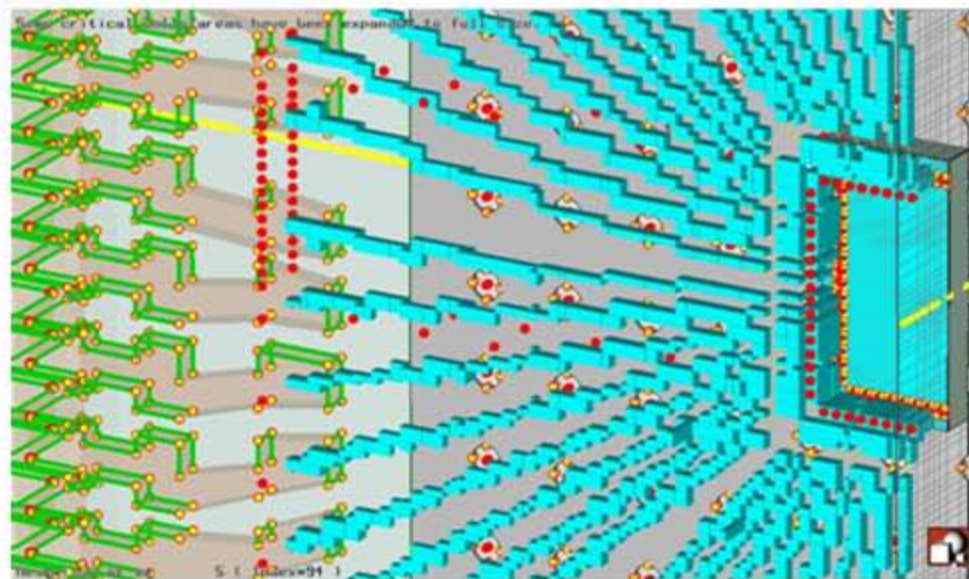
# Meshing Issue

- Choosing improper mesh settings will lead to coarse meshcells
- Cells will be filled with PEC material and produce numerous short circuits in the structure
- Solid wires transposed by infinitely thin wires
- Spatial sampling rate raised (20) and additional mesh step width (0.001 mm) specified for the wires => 10 mil. meshcells



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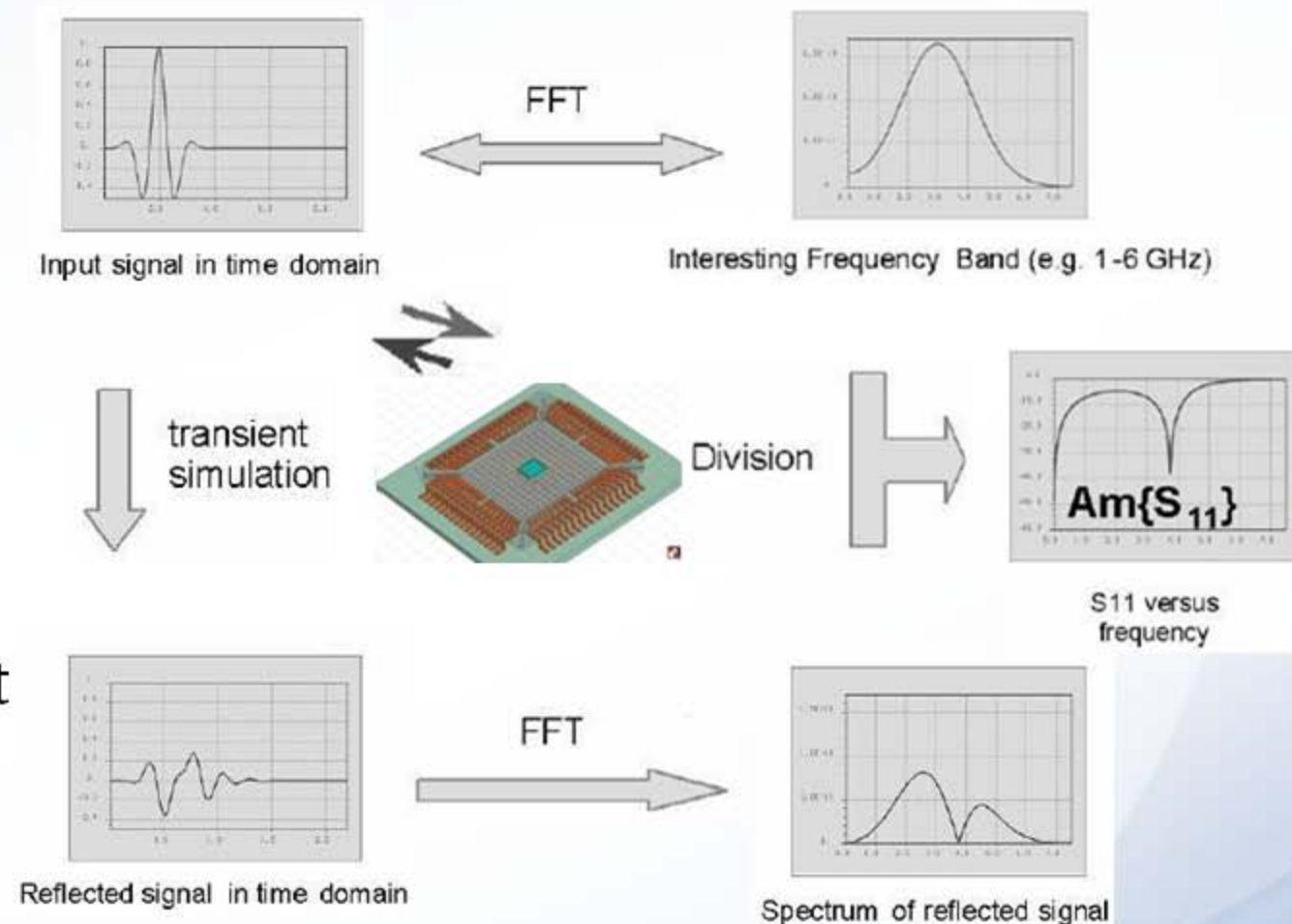
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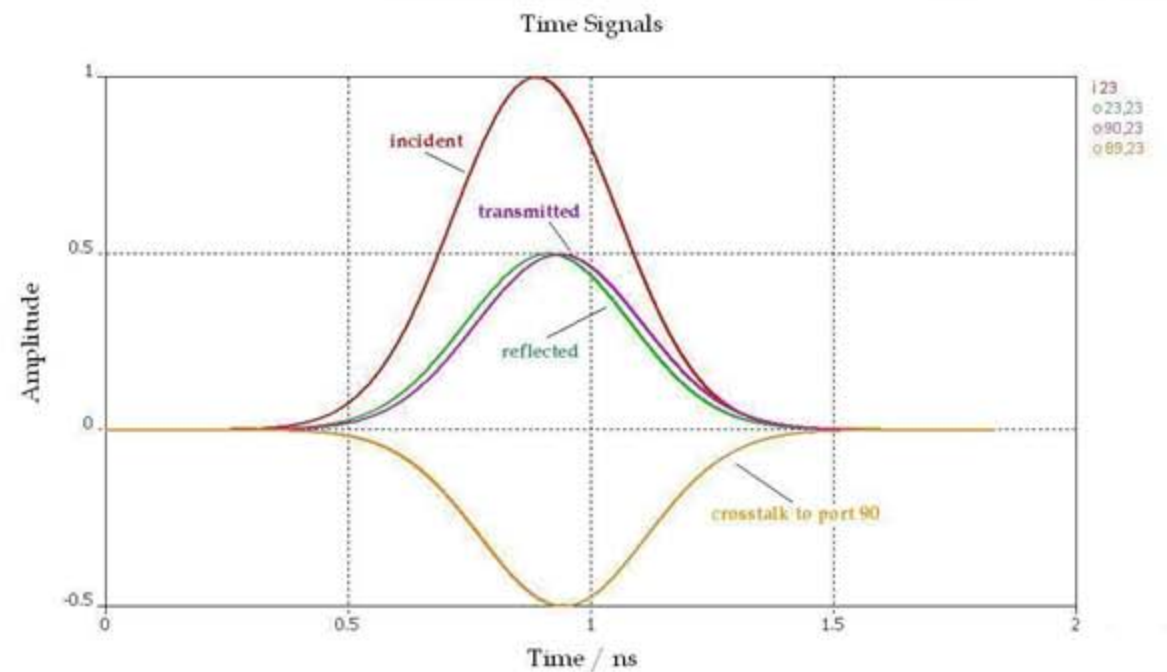
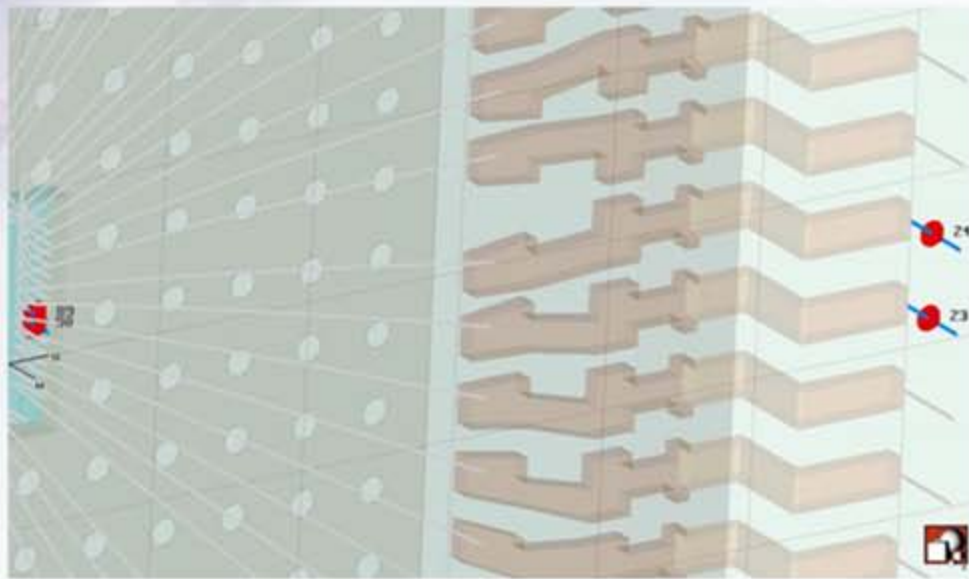


# Solver Types

- Two different solver types were utilised
- Transient solver calculates propagation of electromagnetic fields over time at discrete locations and at discrete time samples
- Frequency solver solves the problem for a single frequency at time



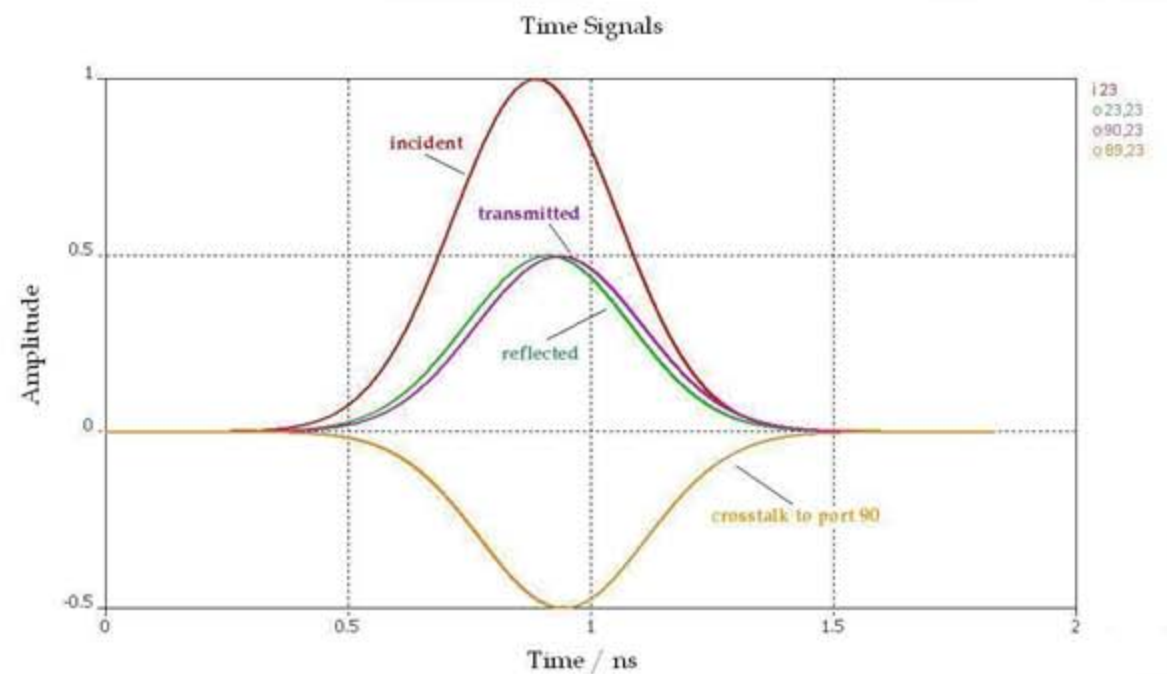
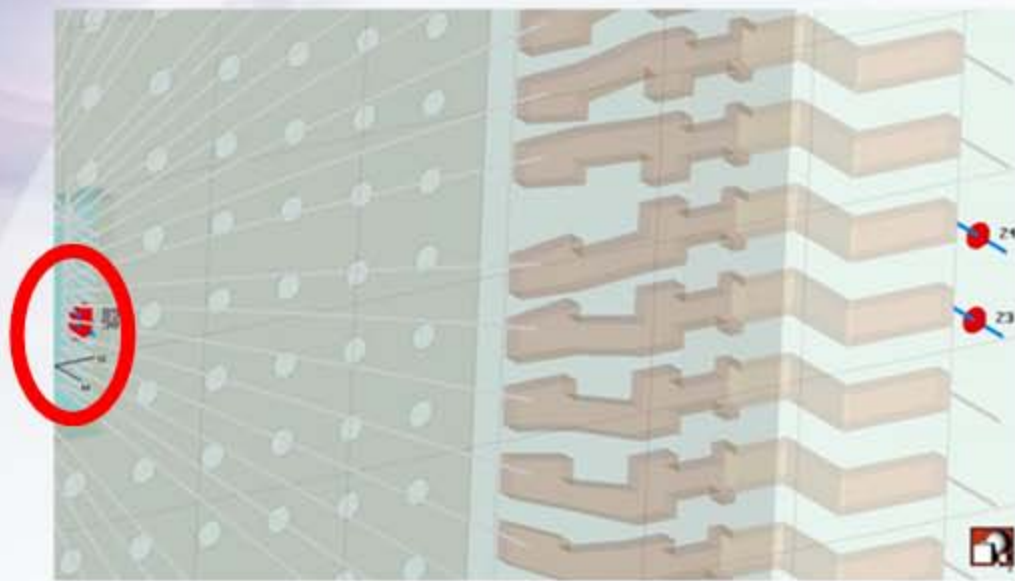
# Simulation Results of Whole Model



- Transient solver was used to analyze signal transmission and to obtain s-parameters
- Signal excitation was performed on two innermost ports and their opposite outermost ports
- Signal curves and s-parameters showed an unusual transmission behavior



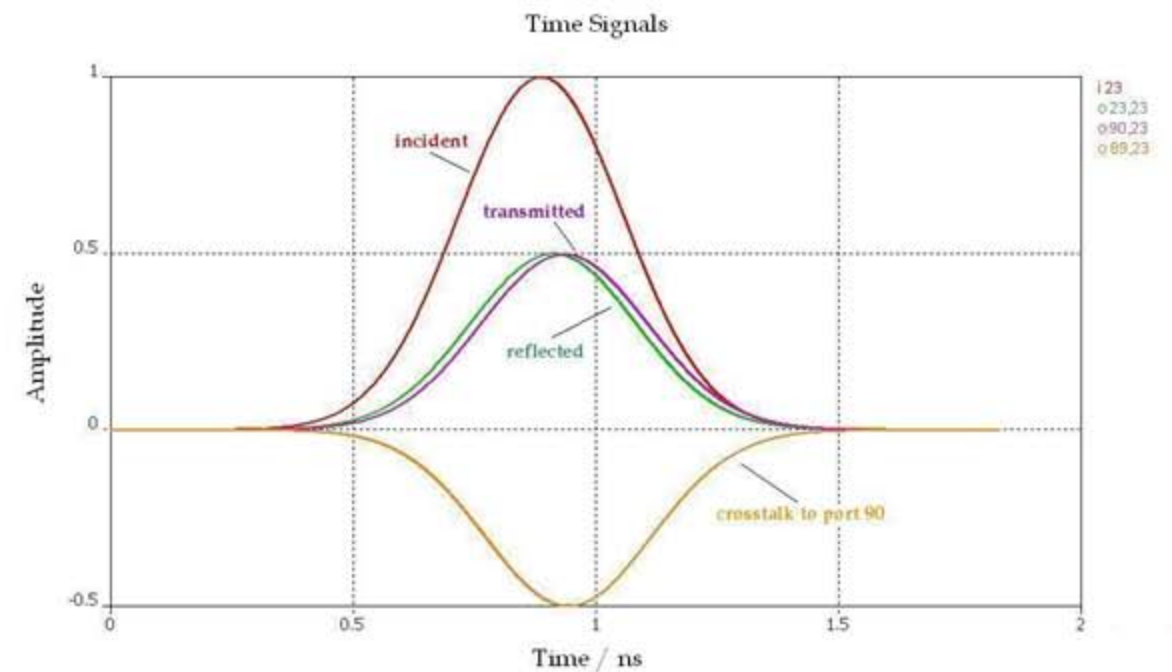
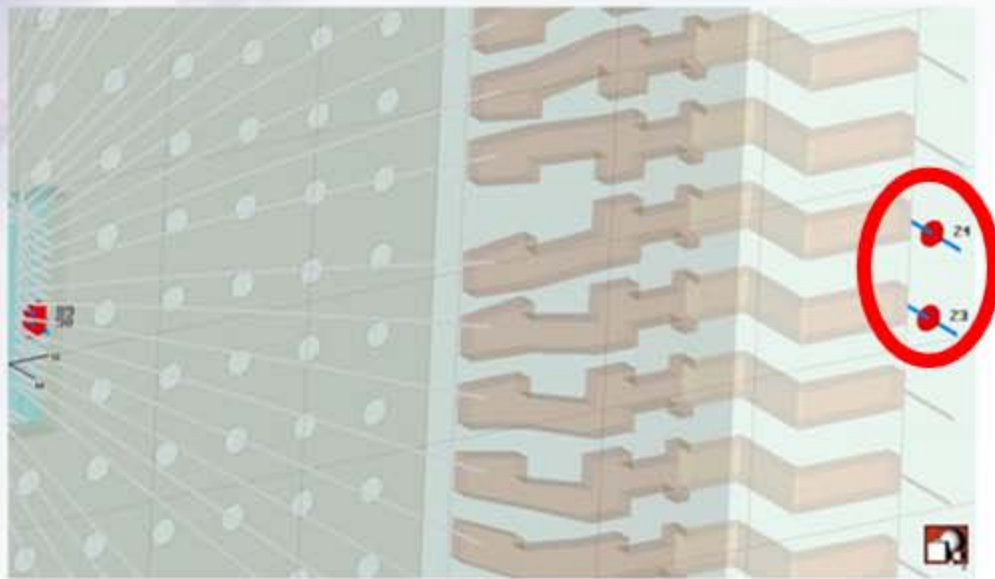
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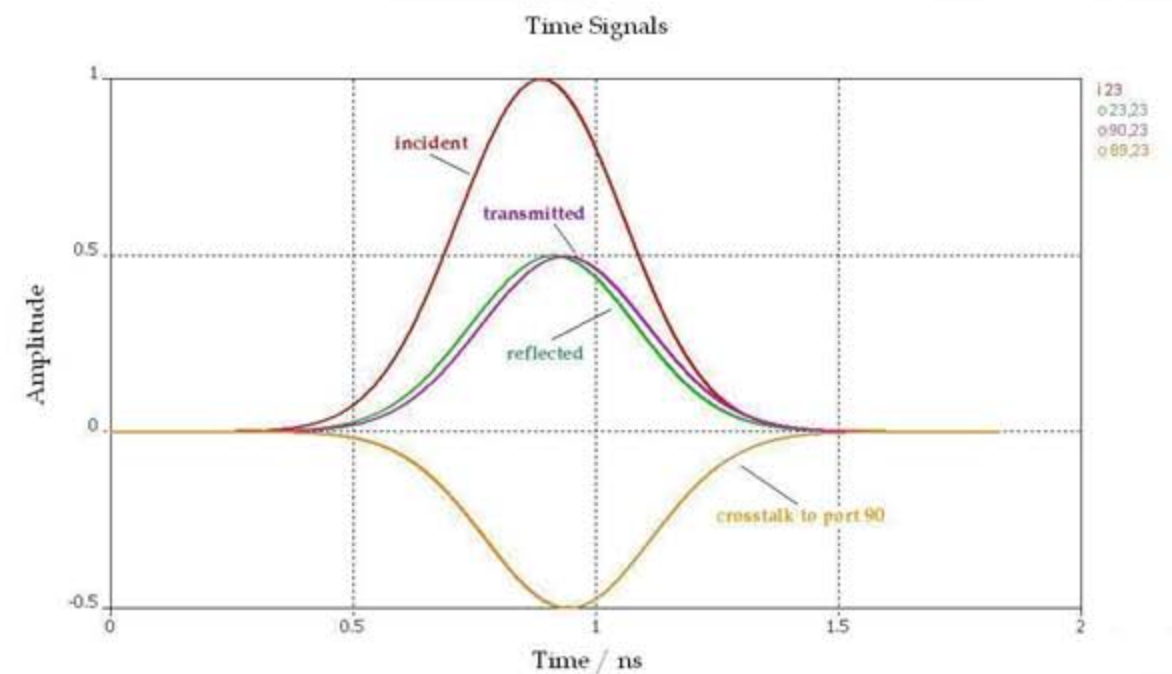
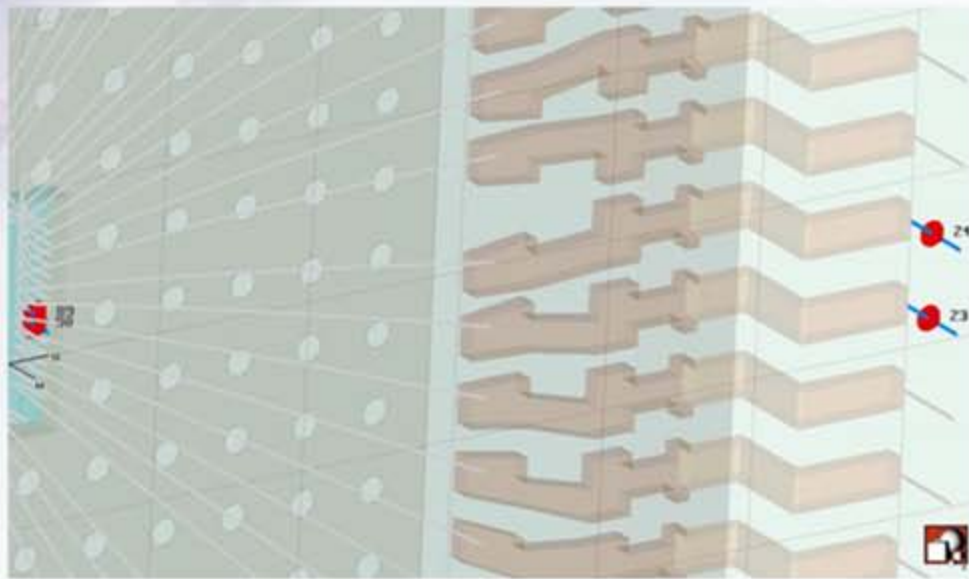


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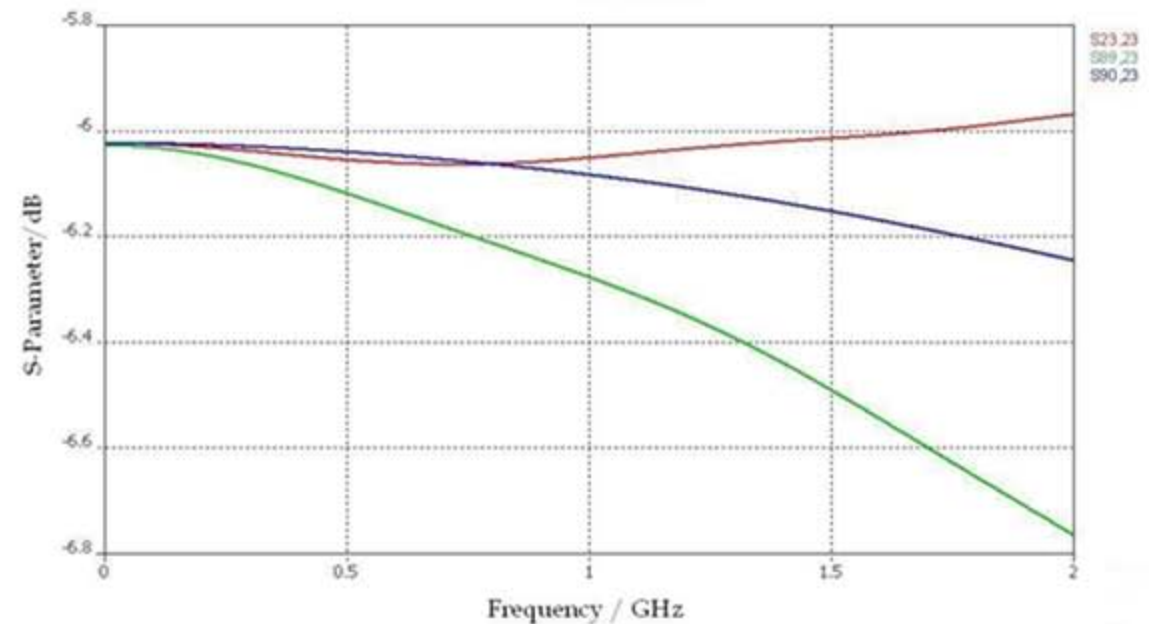
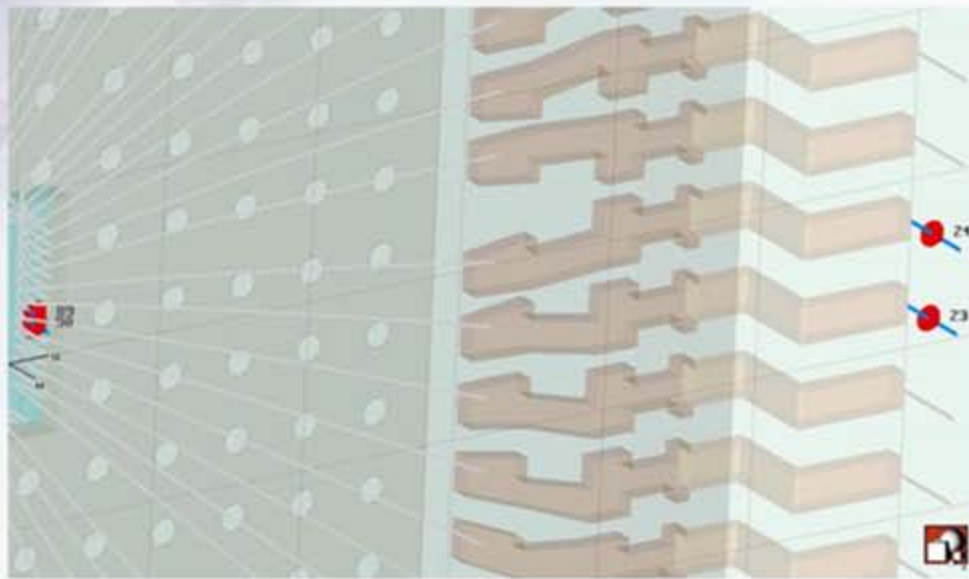
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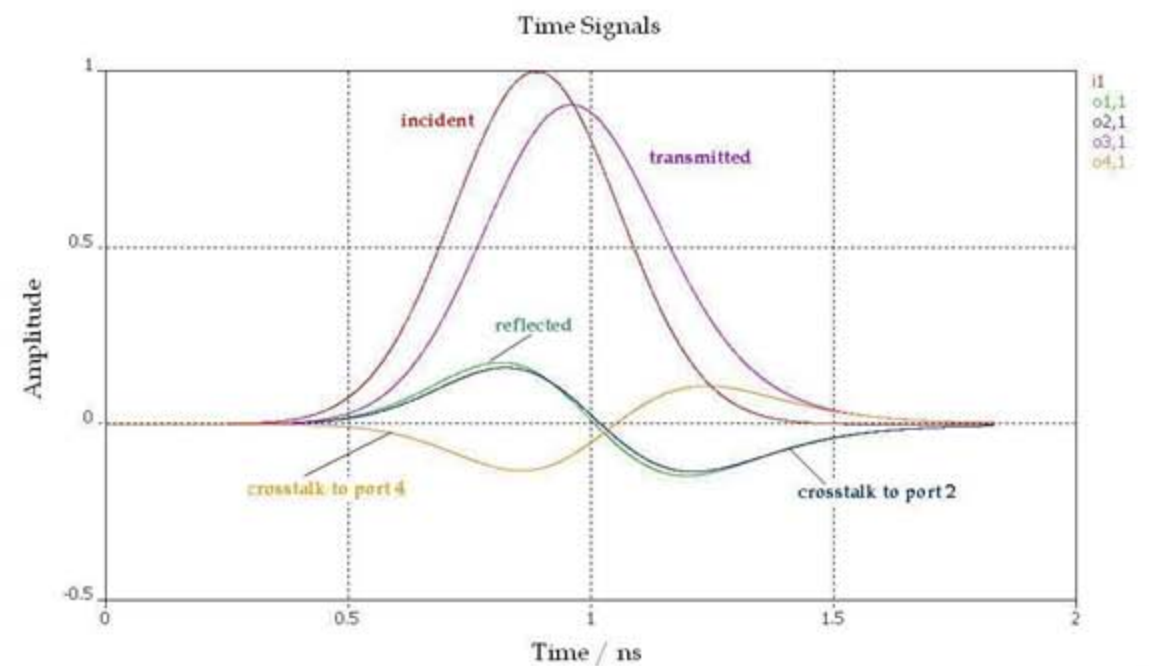
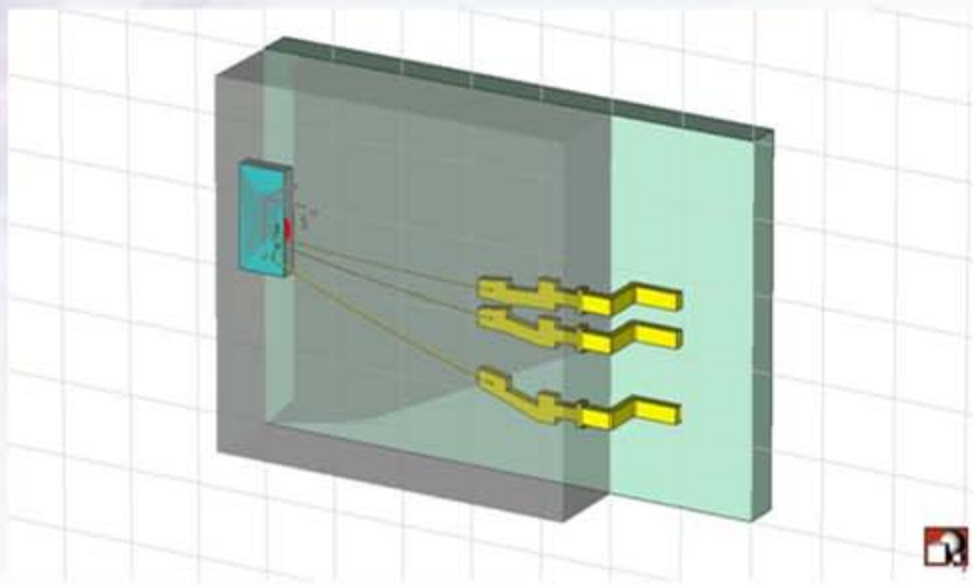
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# Simulation Results of Small Model

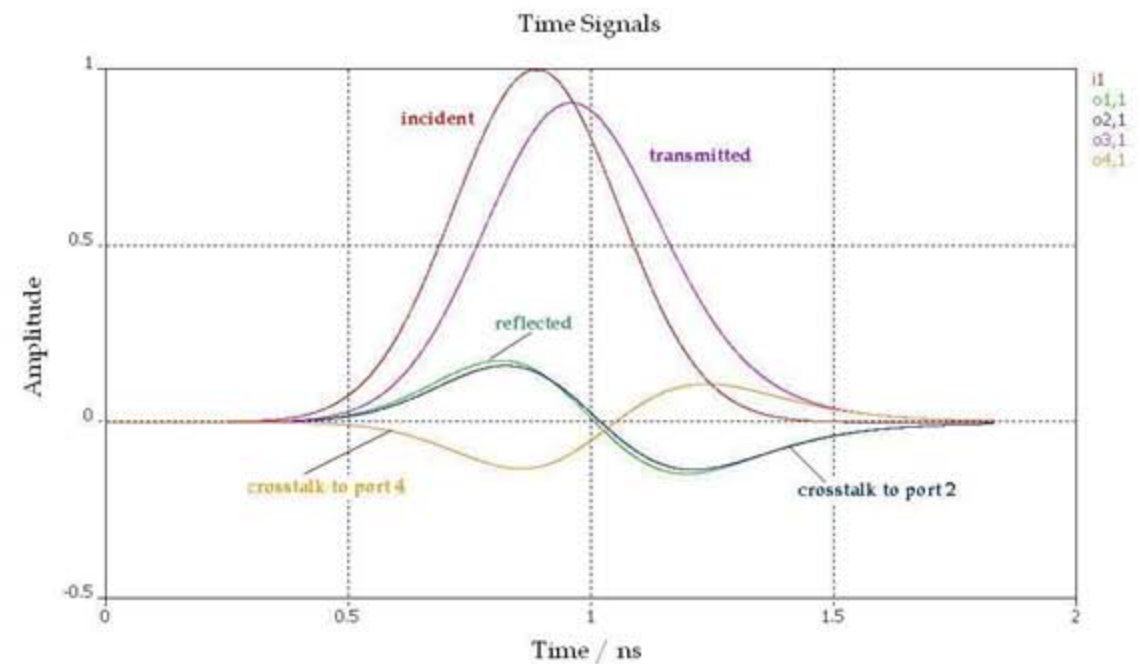
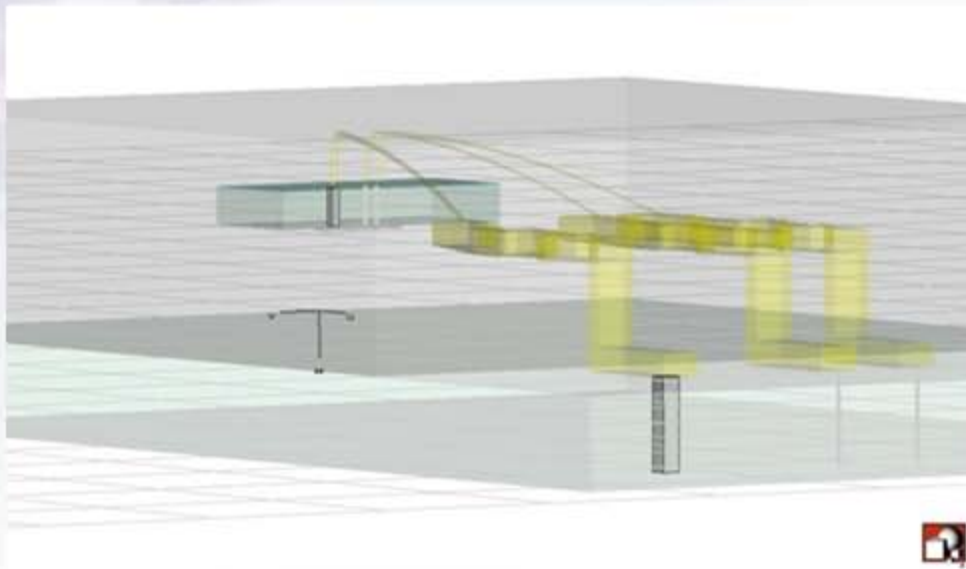


- Smaller model with dimensions of  $5 \times 5 \text{ mm}^2$  consist of a quarter of the whole package.
- Contains two signal leads and an additional lead which is used as a ground lead connecting both ground planes.
- Signal curves and S-parameters show a comprehensible transmission behavior of the structure.





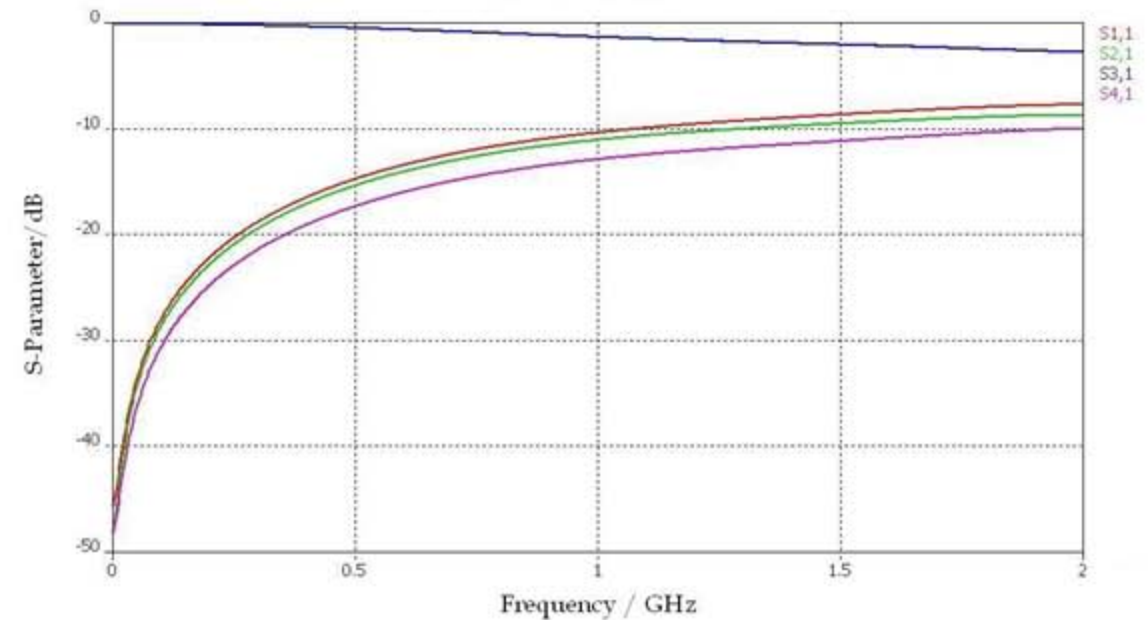
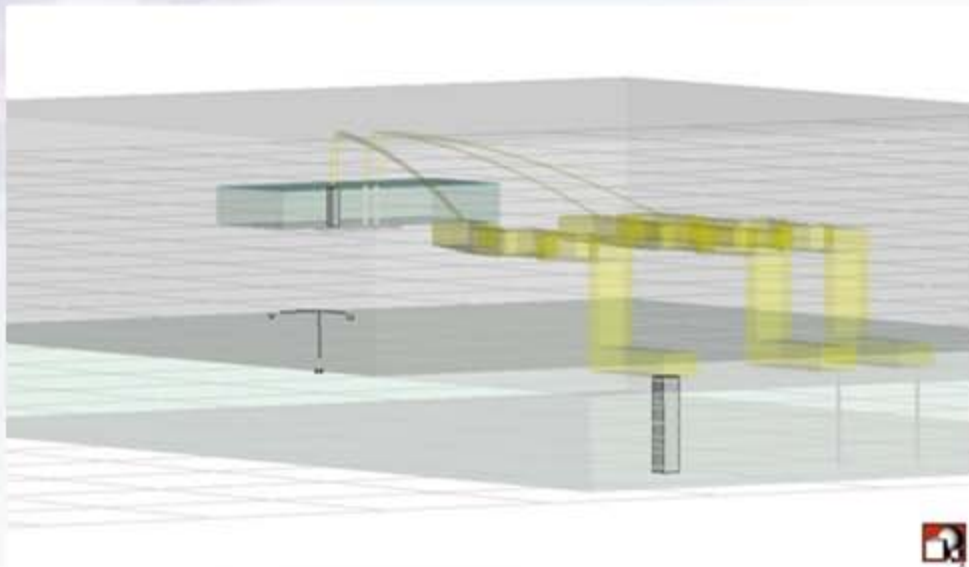
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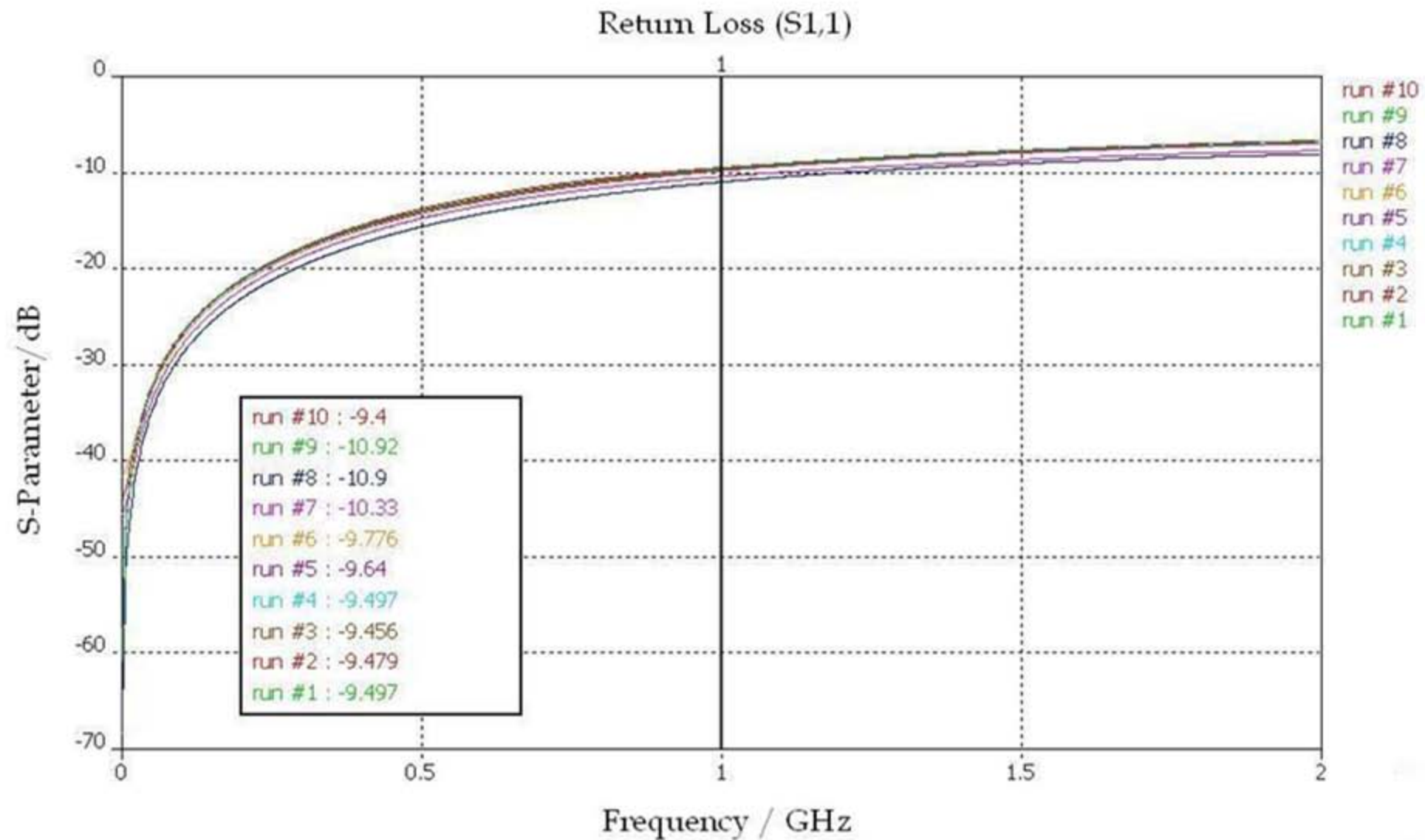
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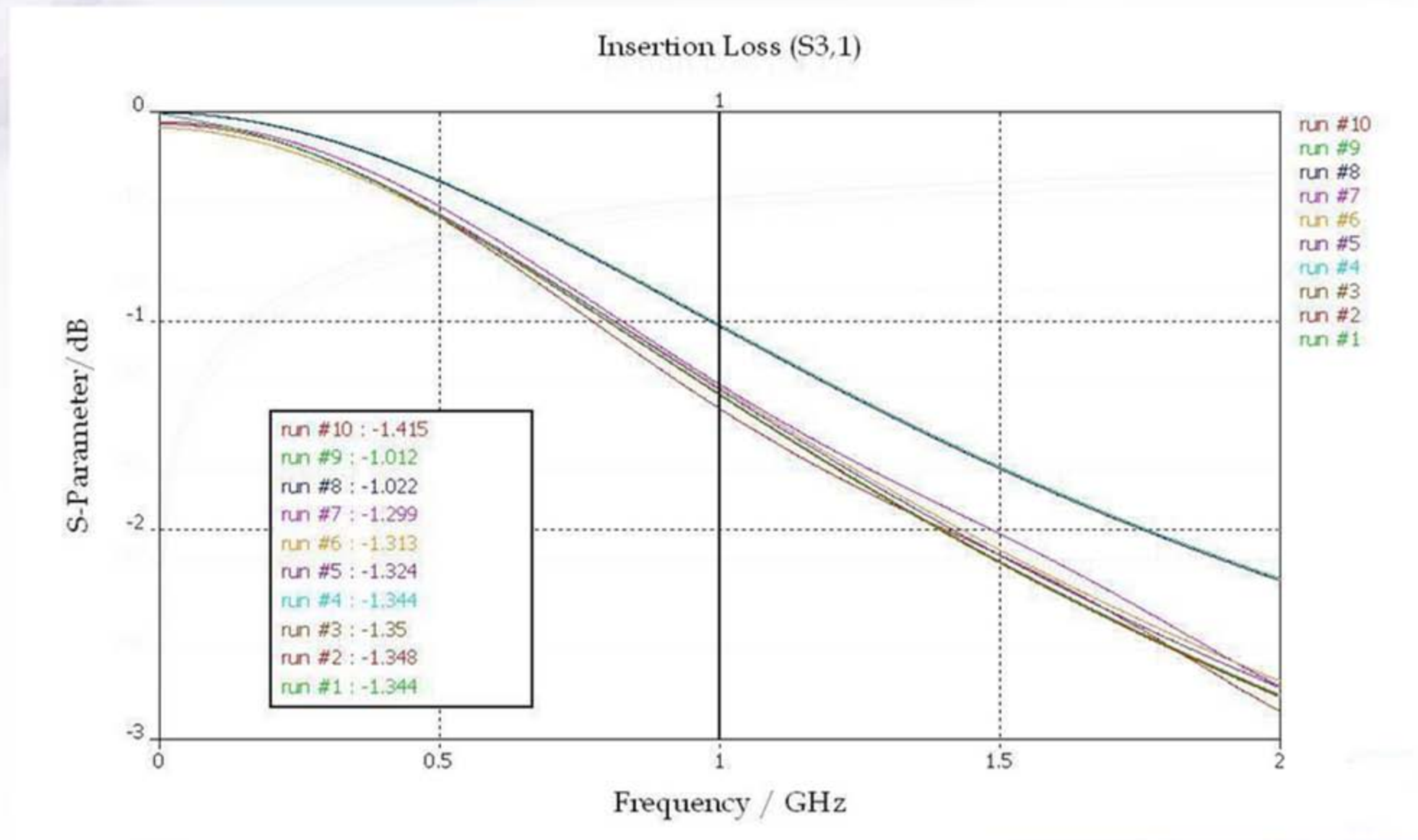
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# Different Simulation Runs

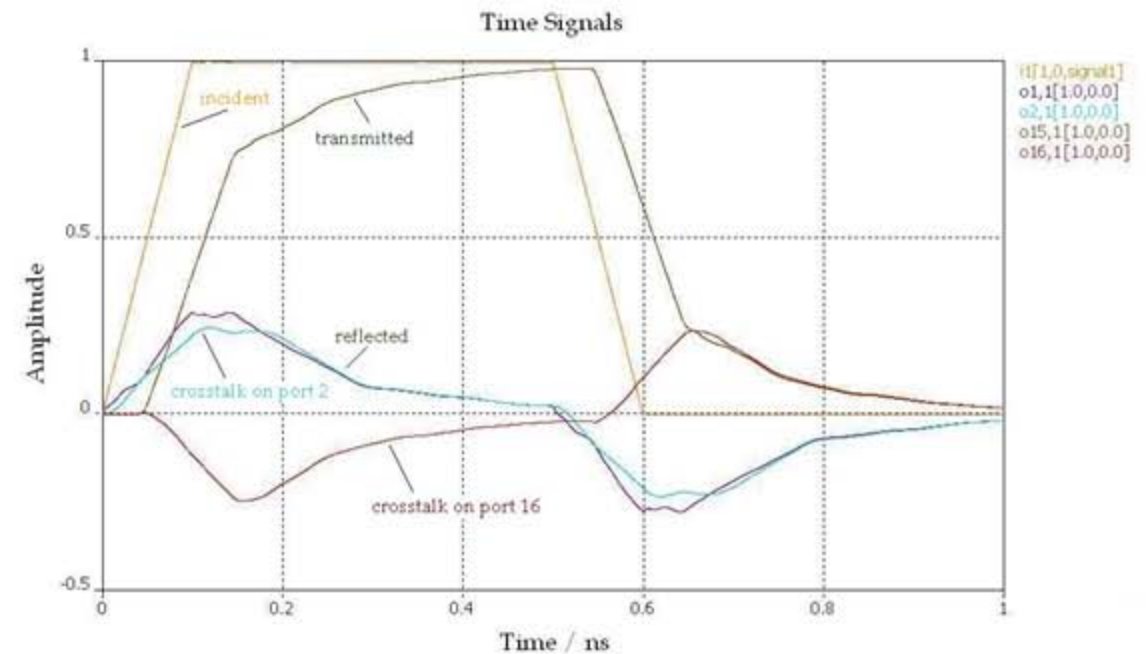
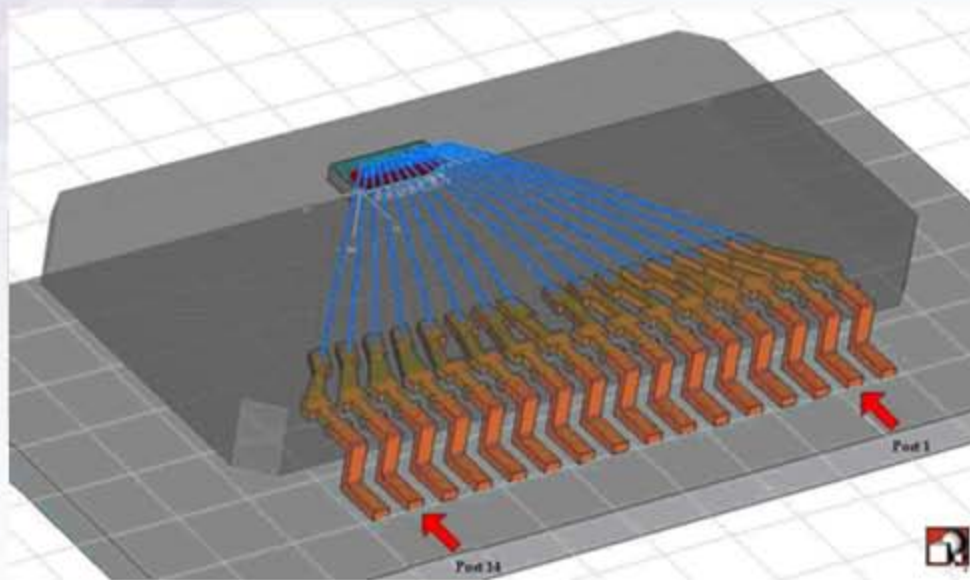


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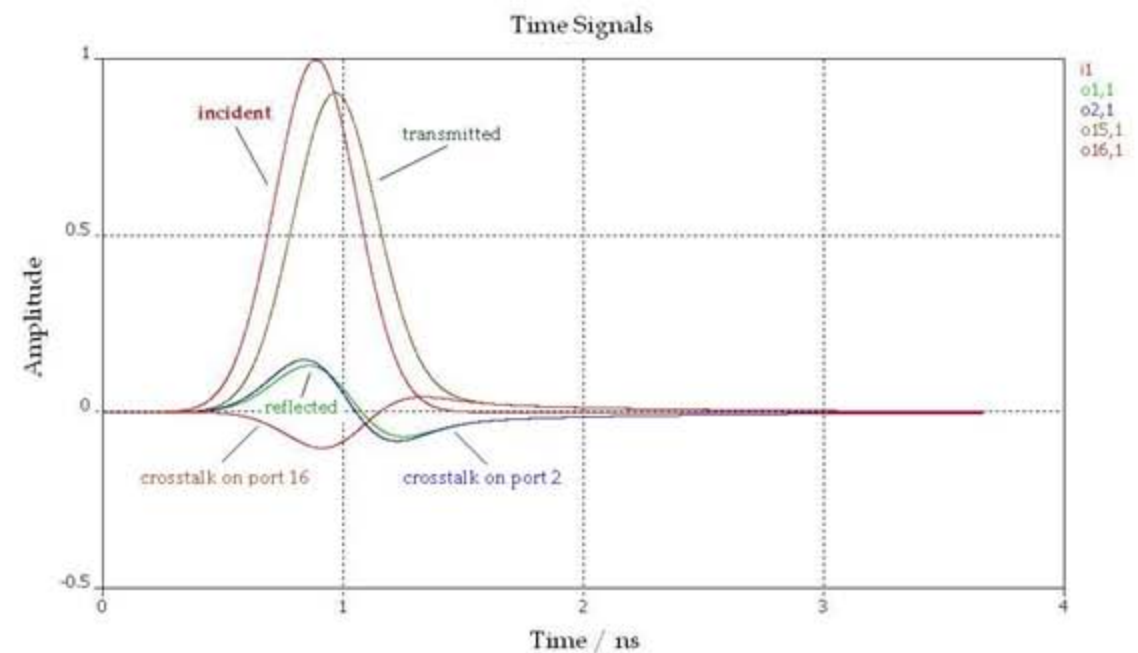
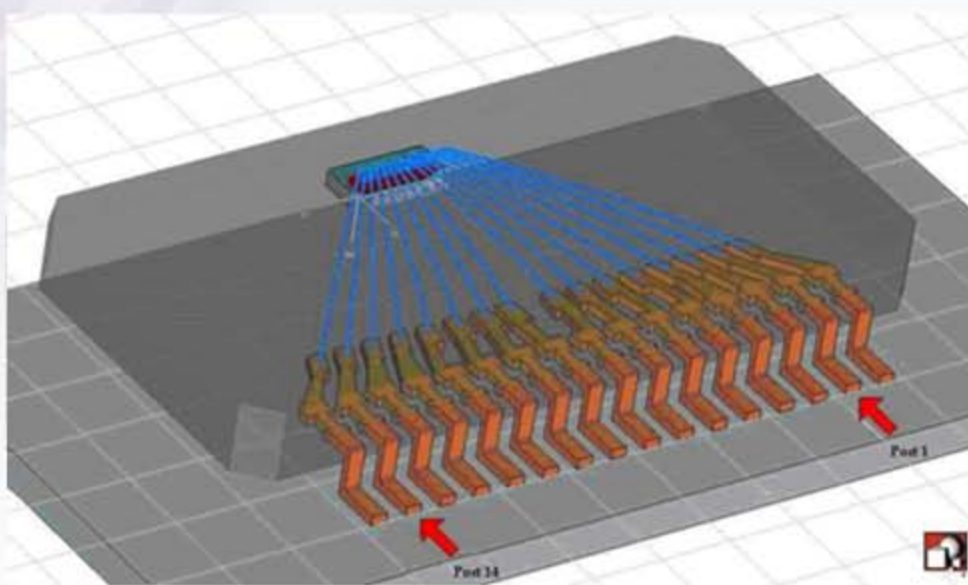
HFT

# Simulation Results of Final Model



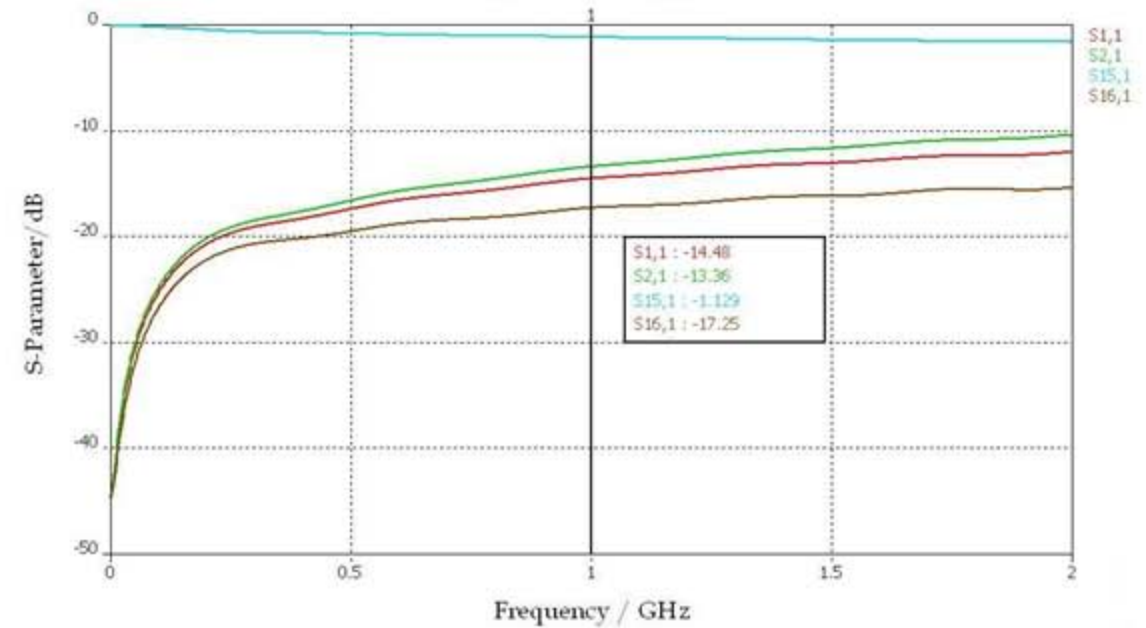
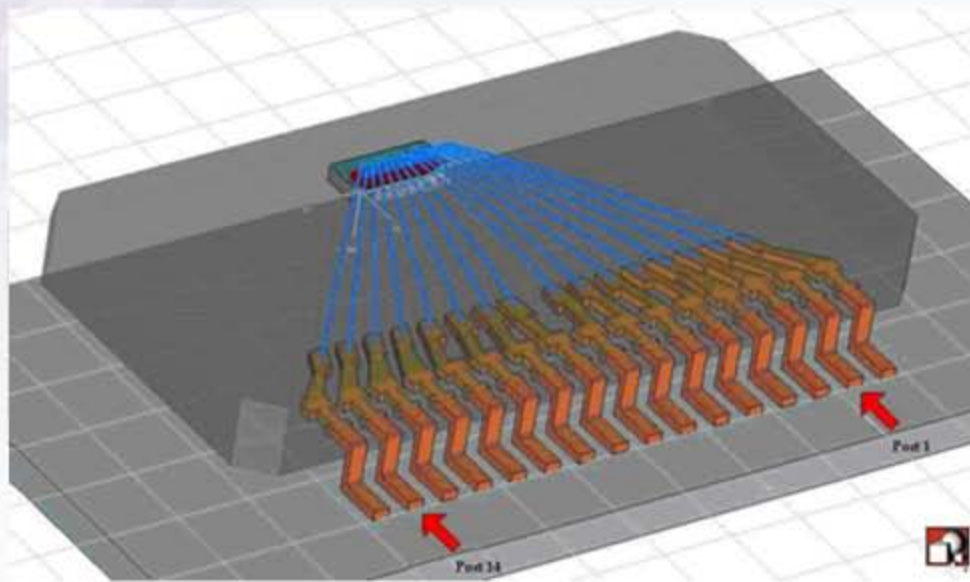
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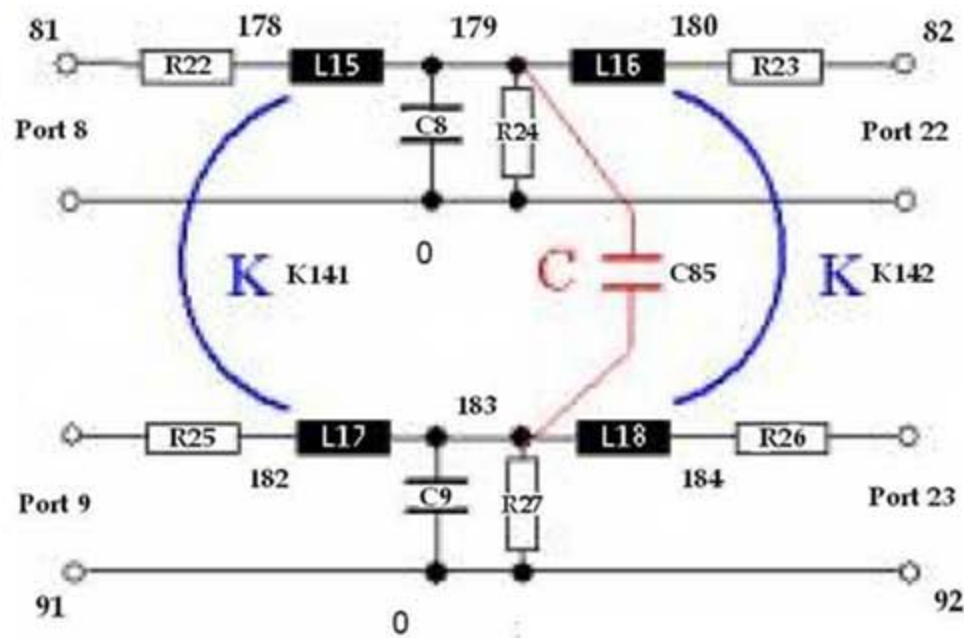
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# Simulation Results



Frequency	1 MHz		1 GHz	
	Infinetly thin wires	Solid wires	Infinetly thin wires	Solid wires
<b>R22-R23</b>	0.02Ω	0.42Ω	2.13Ω	5.06Ω
<b>L15-L16</b>	3.8nH	4.3nH	2.19nH	3.8nH
<b>C8</b>	0.33pF	0.29pF	0.066pF	0.259pF
<b>R24</b>	0.4GΩ	1GΩ	10kΩ	4.1kΩ
<b>R25-R26</b>	0.02Ω	0.42Ω	2.20Ω	5.19Ω
<b>L17-L18</b>	4.2nH	4.71nH	2.2nH	4.21nH
<b>C9</b>	0.29pF	0.27pF	0.068pF	0.231pF
<b>R27</b>	0.7GΩ	2GΩ	10kΩ	3.7kΩ
<b>K141-K142</b>	2.5nH	2.8nH	2nH	2.7nH
<b>C85</b>	0.3pF	0.27pF	0.27pF	0.249pF





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# Summary & Outlook

## Modeling :

- X-ray close-ups were taken in order to facilitate a precise modeling.
- Several 3D models were created using CST MWS.

## Simulation :

- Meshing and ground issue was solved so that appropriate signal waveforms and s-parameters were facilitated. Most suitable trade-off was obtained, thus best one was chosen to perform a final simulation on a sufficient model.
- For each run T-shaped equivalent circuit was extracted at 1 MHz and 1 GHz.
- Results obtained for 1 MHz show good agreement with literature; no comparable results have been found for 1 GHz.

## Outlook :

- Investigating the input of package parasitics on the signal integrity in SPICE.
- With the developed methodology more complex packages can be investigated.



**Thank you for your attention !**



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